EE 432/532 — CyMOS process

NMOS source/drain diffusion

In this lab, we perform the entire the NMOS source/drain phosphorus diffusion – cleaning, deposition, and drive. As with the PMOS source/drain diffusion doe previously, we want a relatively high doping concentration (high dose) and relatively shallow junction. The high doping in the source/drain regions helps to make better contacts and reduces overall device resistance.

Design the diffusion so that the surface concentration will be approximately $5x10^{19}$ cm^{-3} and the junction depth will be approximately 0.75 µm. Note that the diffusion coefficient for phosphorus is not well modeled by a single-value Arrhenius number. The diffusions tend to go deeper than the simple model predicts. As we have done before, we will grow approximately 0.25 µm of oxide at the beginning of the drive step.

Before Lab

1. Read through the *Phosphorus Deposition* SOP. There is no SOP for phosphorus drive — the drive can be treated as a regular wet oxidation process, very similar to the boron drive. However, there is no low-temperature oxidation needed after the phosphorus deposition.
2. Read through the manufacture's data sheets for the phosphorus source wafers. Note that we have the PH-950 source wafers. (The link to the product data is on web site.)
3. Read through the NMOS diffusion pages of the *CyMOS Process Traveler*.
4. Choose a deposition temperature in the range of 875°C to 925°C. The deposition time (t_1 > 45 min) and the drive time and temperature should be chosen to meet the diffusion profile requirements.
5. Calculate the required oxidation time, using the temperature chosen for the drive.

Activities

1. Photograph patterns formed during the previous lithography step. (Suggested photos subjects: alignment marks, a few PWELL rectangles with the added NMOS S/D openings, a few PMOS regions showing the added substrate contacts, new vdP and TLM patterns, BJT regions, NAND and NOR gate regions, anything unusual.)
2. Measure the PWELL sheet resistance on test wafer 1 using the four-point probe setup. Do a 4x4 wafer map of the sheet resistance — similar to the wafer map done with the thickness oxide — to see the variability across the wafer.
3. Perform a standard clean on all of the wafers.
4. Load the wafers into the phosphorus furnace and perform the phosphorus deposition. Make sure that you use the correct tube (the top one) and the correct temperature controller (Zones 1 – 3 of the left-hand controller).
5. Remove the wafers and deglaze for 30 seconds. Then rinse and dry.
6. Load the wafers into the oxidation furnace and perform the oxidation/drive.

7. Remove the wafers and measure the oxide thickness on all wafers. (If needed, it is OK to leave the wafers in the furnace for the next group to remove, and then measurements can be done next time.

Comments

1. As discussed in class, when using the four-point probe measurements, we can only determine sheet resistance for the PWELL — this is diffusion profile, so there is no single value of resistivity that makes sense. As we learned in class, the sheet resistance of a dopant profile is essentially an average value of the resistivity.
2. Doing 16 four-point probe measurements will be bit time consuming. You can divide the effort in order to work more efficiently. One person can set the currents, one person can record the voltages, one person can move the wafer and set the probes. If it is a four-person team, the fourth person can begin preparing the standard clean.
3. To ensure adequate phosphorus dose, the deposition time should be at least 45 min.
4. The phosphorus drive is done in the oxidation furnace.
5. The total deposition time should include the push and pull time. Because of the relative fast diffusion of phosphorus in silicond, we speed up the push/pull rates for moving wafers in and out of the phosphorus furnace.
6. Note that the junction is between the phosphorus diffusion profile and the boron diffusion profile of the p-well diffusion, so you will have to modify the junction depth equation to handle that.
7. It's a busy week, so start early if you can and plan for the possibility of having to stay late. Multi-tasking (dividing up the work) is strongly suggested.
8. The next step — gate oxide patterning — will be done by the lab instructors.

Reporting

Prepare a report that covers the PMOS lithography and the PMOS diffusion (both deposition and drive). The report is due by Apr 3 and should be submitted to Canvas.

At a minimum, the report should include:

- a description of the NMOS steps in terms of the overall CyMOS process
- a summary of the lithography process
- details of the lithography process (photoresist type, spin speed, exposure time, etc.)
- photos of the etched patterns
- a summary of the the boron diffusion deposition and drive steps. (including information from the boron source wafer data sheets)
- calculation of diffusion details (dose, surface concentration, junction depth, oxide thickness, etc.)
- measured oxide thicknesses after the diffusion.
- copies of the completed sheets from the relevant portion of the process traveler. (In an appendix.)