NMOS source/drain lithography

In lab, we will perform the third lithography step to create the openings needed for the NMOS source and drain regions.

Before Lab

1. Review lithography lab instructions (SOPs, general procedures, etc.)
2. Review the mask patterns in the *CyMOS Mask* document.

Activities

1. Measure the oxide thickness from the PMOS source/drain drive finished last week. You do not need to do a wafer map, but be sure to measure several points on each test wafer and calculate an average thickness for each.
2. Perform lithography on all device wafers. (Test wafers are not patterned.)
3. Inspect photoresist patterns.
4. Etch patterns into the silicon dioxide and remove photoresist.
5. Take pictures of patterned wafers.

Comments

1. The procedures are exactly the same as for the PMOS lithography, including the obligatory frustration with alignment.
2. Note that test wafer 3 is used for etch calibration, but test wafer 1 should be included in the etch to remove the oxide. Recall that TW1 has the PWELL diffusion, and we want to do the NMOS diffusion into TW1 as well.

Report

The results of this work will be combined with the work of the next lab (NMOS source/drain diffusion) into a single report. Be sure to record all relevant process information during the lithography (spin time & speed, exposure time and intensity, develop time, etch time, etc.) to include in the report.