EE 432/532 — CyMOS process

PMOS source/drain lithography

In lab, we will perform the second lithography step to create the openings needed for the PMOS source and drain regions.

Before Lab

1. Review lithography lab instructions (SOPs, general procedures, etc.)
2. Review the mask patterns in the *CyMOS Mask* document.
3. Immediately prior to lab, spend 30 minutes in meditation to bring yourself into the right frame of mind before coming to grips with the dreaded alignment procedure.

Activities

1. Measure the oxide thickness of the test wafers from the p-well drive. You do not need to do a wafer map, but be sure to measure several points on each wafer and take an average.
2. Perform lithography on all device wafers.
3. Inspect photoresist patterns.
4. Etch patterns into the silicon dioxide and remove photoresist.
5. Take pictures of patterned wafers. (Probably deferred until the beginning of the next lab period, unless you finish very quickly this week.)

Comments

1. The procedures are exactly the same as for the p-well lithography, with the added requirement of alignment.
2. Alignment can be frustrating. Your lab instructor will show you some tricks for achieving the alignment with minimal mental anguish. Familiarity with the layout of the mask patterns will also help, so you might want to look over the mask patterns before-hand.
3. Instead of using the ovens for the pre- and post-bake, we will switch over to use hot plates, which are faster. The short times makes the process somewhat more error-prone, and checking the photoresist carefully before etching is even more essential.

Report

The results of this work will be combined with the work of the next lab (PMOS source/drain diffusion) into a single report. Be sure to record all relevant process information during the lithography (spin time & speed, exposure time and intensity, develop time, etch time, etc.) to include in the report.