EE 432/532
CyMOS process

PWELL lithography

We perform the first lithography step to create the openings needed for the PWELL regions.

Before Lab

1. Read the "Litho & etching overview" notes on the web site.
2. Read the instructions for operating the Filmetrics system for measuring oxide layers.
3. Read through the *Photolithography* SOP.
4. Review the PWELL litho page of the *CyMOS Process Traveler*.
5. Take a preliminary look at the mask patterns given in the mask pattern notes.

Activities

1. Measure the oxide thickness of the wafers that were oxidized last time.
2. Perform lithography on all device wafers. Note that the test wafers are *not* patterned.
3. Inspect photoresist patterns.
4. Etch patterns into the silicon dioxide and remove photoresist.
5. Take pictures of patterned wafers. (Probably deferred until the beginning of the next lab period, unless you finish very quickly this week.)

Comments

1. Measure the thickness of the oxide grown last week with the Filmetrics system. Perform a *wafer map* on test wafer 1, measuring at least sixteen points on the wafer surface. (There are some blank maps in the lab or you can download one from the web site.) Then measure at least one point on each of the remaining test wafers. (Remember, this is data that goes into the *first* report, not the second.)
2. This week, when we do the pre- and post-bake steps for the photoresist, we will use the ovens rather than the hot plates. The pre-bake oven should be set at ≈ 80°C. The pre-bake time is 25 minutes. The post- bake oven is set at ≈ 120°C, and the post-bake time is 20 min.
3. The lab instructor will explain the use of the test wafer to determine the correct etching time.

Report

The results of this work will be combined with the work of the next lab (PWELL diffusion) into a single report. Be sure to record all relevant process information during the lithography (spin time & speed, exposure time and intensity, develop time, etch time, etc.) to include in the report.