EE 432/532 — CyMOS process

Device testing

Now comes the pay off after all these weeks of work — we learn if our transistors and other devices actually work. We have two weeks to complete the testing. (And perhaps a third, if necessary.) This is a short synopsis of events.

1. Learn how to use the probe station to make connections to device contacts.
2. Choose a one device wafer from the group's batch as the "prime candidate".
3. Make a preliminary measurement of the p- and n-type contacts.
4. Sinter the wafer in the small furnace.
5. Re-test the contacts to see if they are improved.
6. Perform TLM measurements on the contacts to the PWELL, PMOS, and NMOS diffusions.
7. Take current-voltage measurements from at least two diodes.
8. Collect current-voltage measurements from representative NMOS and PMOS transistors on the wafer.
9. Measure device parameters from all of the NMOS and PMOS wafers from one die on the "prime wafer".
10. Measure the capacitance-voltage curve from the p- and n-type capacitors on the die.
11. Measure a parameter from one representative device from each die on the wafer to make a wafer map.
12. Perform any optional measurements: van der Pauw, BJT, logic gates, etc.
13. Collect wafers, lab coats, and goggles to take home.

Parameter analyzer

Transistor and other device testing makes use extensive use of the parameter analyzer in the lab. The model we have is an old HP 4136. It is similar to the B1500 parameter analyzer used in the EE 230 and 330 labs, but it is a few decades older. (The floppy drive on the front is a clue to its age.) Even though the unit is old, the measurement hardware is still perfectly good, and the machine works well for our needs.

There are detailed instructions on the web site describing the use of the parameter analyzer in manual mode to collect data. We may use the analyzer in manual mode to do some measurements.

In the past few years all measurements were done manually, and we "collected data" by taking pictures of the I-V graphs on the analyzer. This year, thanks to Poly, we will have computer control over the analyzer, and we will be able to import device measurement data into the computer for analysis and to make nice graphs, instead of trying to do everything using crappy photographs. Poly's software is at the beta stage (maybe pre-beta), and there may be some rough edges. If so, we can work those out as we go along. But data collection this semester will be much better than in past years.

Contacts & sintering

Start by taking preliminary measurements of a few resistors on the wafer. You can use TLM resistors or van der Pauw patterns for this initial probing. Measure both p-type (PMOS S/D diffusion) and n-type resistors (NMOS S/D diffusion). It is likely that the *I-V* characteristics will be non-ohmic initially because the contacts are not complete. Be sure to record at least one n-type and one p-type curve from these initial measurements.

After the preliminary resistor measurements, contact *sintering* should be done in the small tube furnace for 15 minutes at 4025°C with a nitrogen flow of 1 slpm. (The furnace temperature and flow should be set, so all that is needed is to move the wafers in and out.)

After sintering, re-measure the resistor *I-V* curves. (The curves should be more linear than before sintering.) Again, record *I-V* characteristics for n-type and p-type devices.

Device measurements

Pick one wafer from your group's collection. All of your measurements should come from this wafer. You might need to do some trial-and-error probing to find a wafer that has lots of working devices. Even though the "official" measurements will focus on one wafer, you can certainly do extra measurements on other wafers if you have time and interest.

Then focus on one die on the wafer and perform the following measurements. (Again, you may want to probe around a bit to determine which die has the most working devices.)

Diodes

Check the operation of several diodes. One easy place to access diodes is between the drain and substrate contacts of any of the MOSFETs. You could also look at the base-emitter and base-collector junctions of the bipolar junction transistors. Record at least two sets of diode *I-V* curves. Be sure to look at the reverse breakdown voltage as well as the forward characteristics. (Not all diodes will have low breakdown voltages. For instance, the B-E junction of a BJT will have much lower breakdown voltage than the B-C junction. Similarly, the drain-substrate junction of the NMOS transistors will have lower breakdown than that of a PMOS. Those of you with a bit more training in device theory can probably explain this behavior.)

TLM measurements

Measure the resistance values for all of the contacts on the transfer-length-method (TLM) resistors. Use the measurements to determine the sheet resistance and contact resistivity for the p- and n- diffusions. (TLM1 has n-type contacts in the NMOS source/drain diffusion, TLM2 makes contact to the PMOS source/drain diffusion, and TLM3 makes contact to the pwell.)

NMOS transistors

For at least three of the NMOS transistors (one each of the 5-, 10-, and 20-micron length gates), record a set of I_D vs. V_{DS} curves for at least five values of V_G beyond the threshold voltage. Also, record a $(I_D)^{1/2}$ vs. V_{GS} curve. From these measurements, determine V_T and $K = 0.5\mu_n C_{ox}(W/L)$ for the transistors. Measure these parameters for the other 13 NMOS transistors in your chosen die. Use your results to

come up with average values for V_T and $\mu_n C_{ox}$.

PMOS transistors

Repeat the NMOS measurements above for the PMOS transistors.

MOS capacitors

Use the C-V meter to measure the capacitance of the oxide layer, C_{ox} using one NMOS and one PMOS capacitor structure. (Be sure to measure over a range of bias voltages. C_{ox} will be the maximum value measured. Note that C_{ox} is measured in units of F/cm^2. Compare the measured value with the predicted value (based on the gate oxide thickness).

Wafer map

Now expand outside the one die and do a "wafer map" — measuring one property of one type of device for all dice on the wafer. You can measure threshold voltage for a particular MOSFET or C_{ox} using the MOS capacitor structures. As an example, you might measure the threshold voltage for the NMOS with W/L = 20μm/5μm for all sixteen die.

Extra measurements

Depending on the time available, your level of interest, and you measurement skill, you could try measuring the following:

- Van der Pauw measurements.
- I-V characteristics and current gain for the bipolar junction transistors.
- Transfer characteristics for the CMOS inverter.
- Operation of NAND logic gates.

Final report

Prepare a final report for the CyMOS. This will be a group report, not individual. The final report should include all of the processing and testing done this semester. Of course, much of the report writing has already been done in the form of the interim reports. Hopefully, these need nothing more than some editing and revision. The only new lab work in the final report will be the device testing results.

In writing the report, make an effort to tie the various pieces together into a cohesive report. For example, look at the consistency between your estimate of the gate oxide thickness with the measured oxide thickness and the measured gate capacitance.

The final report is due on Saturday, May 10, at the end of finals week. Be sure to keep a copy for yourselves.