EE 432/532 — CyMOS process

Contact lithography

In this lab, we perform the final fabrication step – lithography and patterning of the metal contacts.

Before Lab

1. Review lithography procedures.
2. Review the mask patterns in the *CyMOS Mask* document.

Activities

1. Measure the sheet resistance of: TW1 (which has the NMOS diffusion inside the PWELL diffusion), TW2 (which has the PMOS diffusion), and the aluminum metal layer on one of the device wafers. Measure several points, but a full wafer map is not required for any of these.
2. Perform level-6 lithography on all device wafers.
3. Inspect the patterned photoresist.
4. Etch the patterns using PAN etch.
5. Take photographs of the the patterned wafers.

Comments

- The procedure for measuring sheet resistance of a metal layer is exactly the same as that for a semiconductor layer. Of course, we expect much smaller resistance.
- Alignment is slightly different this time due to the relative transparency of the level-6 mask and the presence of the metal layer, which causes more reflection. It might necessary to reduce lamp intensities when using the microscopes and cameras.
- In order to ensure proper adhesion of the photoresist to the aluminum, we must use the pre-bake and post-bake ovens, as in the first lithography. *Do not use the hot plates for pre- and post-bake!* Without adequate baking, the photoresist patches may break loose from the surface.
- The aluminum etch is a combination of Phosphoric, Acetic, and Nitric acids (PAN). There is no etch calibration required — we will be able to see the etch proceed and can easily observe when it is finished. Each wafer will take 3-5 minutes to etch. Be sure to dispose of the PAN etch in the proper waste bottle.
- Next time: Testing!

Report

Prepare a report the covers the gate lithography, gate oxidation, contact via lithography, metallization, and metal lithography steps. Check the schedule on web site for the due date.