EE 432/532 — CyMOS process

Gate oxidation

This week we will grow the gate oxide. (The lithography for the gate oxide was done by the lab instructors after the NMOS diffusion.) Design the gate oxide growth to achieve an oxide thickness somewhere in the range of 30 nm $\leq t_{ox} \leq$ 60 nm using a *dry* oxidation process.

Before lab

1. Review the SOP for dry oxidation.
2. Pick a time and temperature for the gate oxidation.

In lab

1. If gate oxide patterns have not been etched, do that first.
2. Measure the oxide thickness on test wafers 1, 2 and 4.
3. Photograph patterns formed during the previous lithography step. Suggested photos subjects: alignment marks, a few PMOS and NMOS regions, vdP and TLM patterns, BJT regions, NAND and NOR gate regions, and anything unusual. In addition, take pictures of the gate regions of several different MOSFETs using higher magnification. Examine closely how well the gate overlaps the source and drain regions.
4. Prepare the wafers using the standard clean process. (The last time! Woot!)
5. Load the wafers into the oxidation tube and perform a dry oxidation according to your design.
6. Remove the wafers and measure the oxide thicknesses on all test wafers. (May be delayed until next time.)

Comments

1. TW 4 is the calibration wafer for the gate oxide pattern etch. If the lab supervisor completed the etch before the start of this lab, it will have been etched clean. In that case, there will be no need to measure it.
2. As in previous "hot" labs, the wafers can be left in the furnace once the process is complete. The next group will remove them, and the measurements can be done next week.

Report

The results of this work will be combined with the work of the next two labs (contact-via patterning and metallization and metal contact patterning) into a single report. Be sure to record all relevant oxidation process information during the lithography to include in the report.