Photolithography Mask Documentation

EE432/532

Last Updated: 12 February 2013

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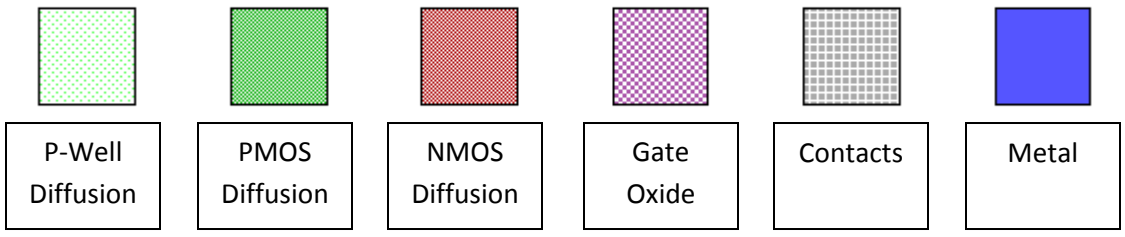
About this Document

This document is a guidance to help EE 432/532 instructors and students to understand the new lithography masks set and mask alignment. This document would contain an overview of the new masks, an introduction of the components the new masks would create, the details of devices on the wafer and their characteristics, and the explanation of the new alignment marks usage.

Color Key



Mask Overview

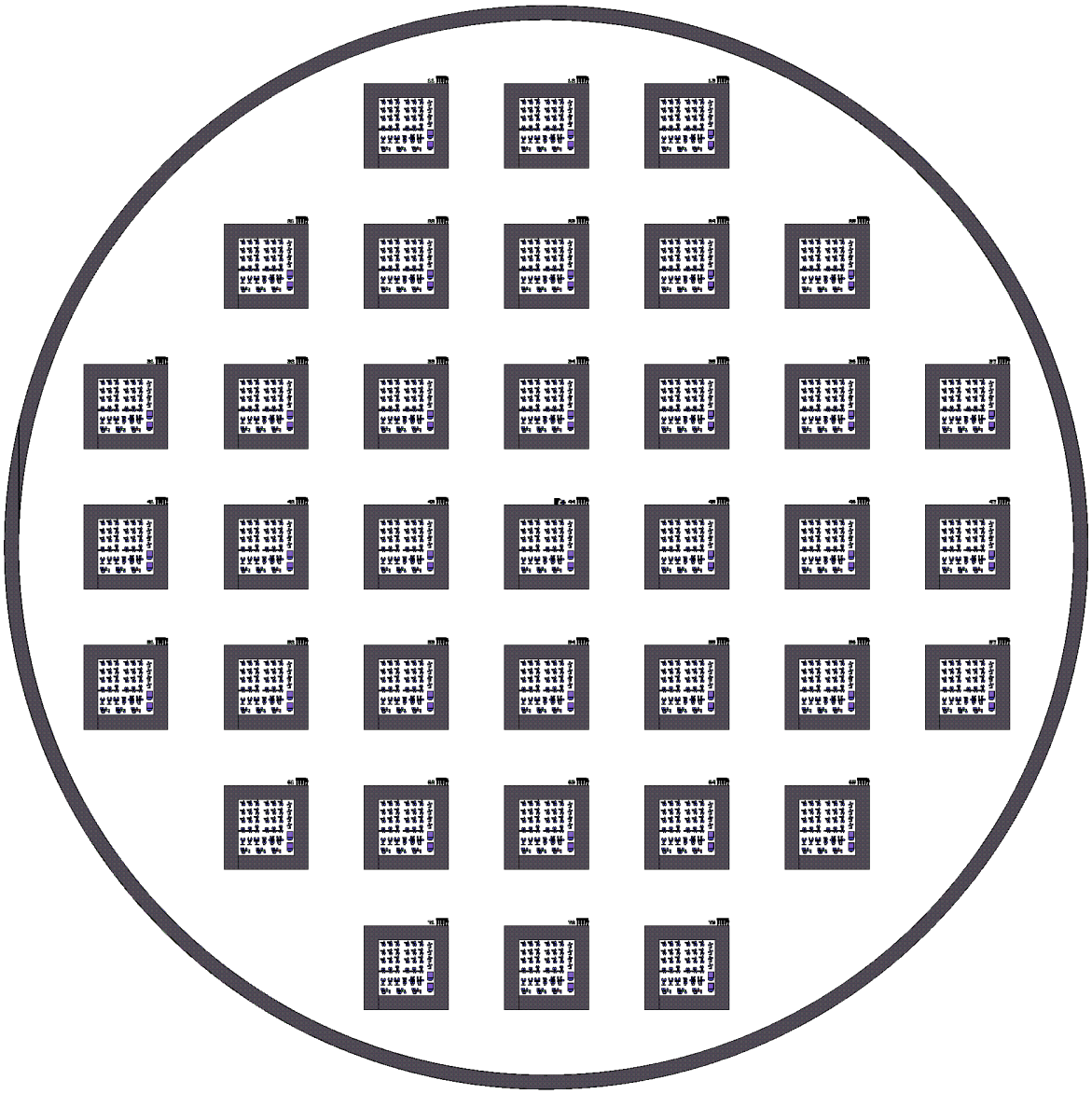


Figure 1: Mask Layout

The photolithography mask for EE 432/532 has 37 dies lined up to be evenly spread out on the wafer. There are 6 individual masks, each used for a different part of the devices. The mask also has a wafer sized ring on it to help with the initial alignment of the mask to the mask aligner.

Die Overview

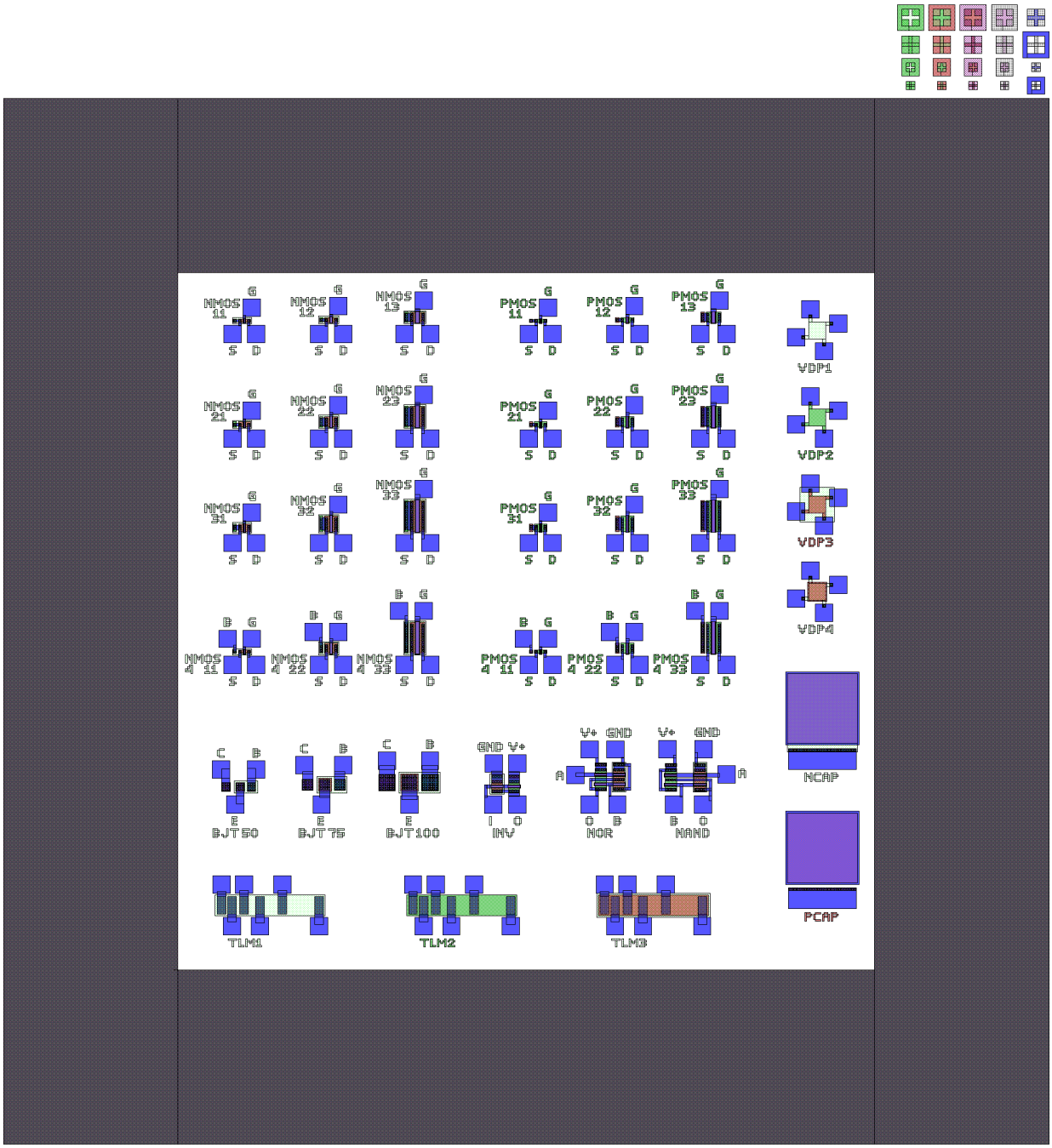


Figure 2: Die Layout

Each die contains a total of 39 devices. The devices are laid out on a grid for ease of numbering. The 3-terminal and 4-terminal transistors in the top left area of the die are number by row and column. The other devices are lined up on the grid on the bottom and right edges of the die.

List of Devices and Sizes

Devices (per die)

Device	# of Devices
3-terminal PMOS	9
3-terminal NMOS	9
4-terminal PMOS	3
4-terminal NMOS	3
NPN BJTs	3
TLM patterns	4
VDP patterns	3
NMOS capacitor	1
PMOS capacitor	1
NAND	1
NOR	1
Inverter	1
Total	39

Sizing

Contacts

All contacts are 10 μm by 10 μm.

Alignment Marks

The top two crosses are 100 μm by 100 μm. The bottom two crosses are 50 μm by 50 μm.

MOSFETs

ID Number	Channel Width (μm)	Channel Length (μm)
11	20	5
12	30	10
13	60	20
21	30	5
22	60	10
23	120	20
31	45	5
32	90	10
33	180	20

NPN BJTs

There are three sizes of BJTs. They are characterized by their emitter area. The sizes are: 50 μm by 50 μm, 75 μm by 75 μm, and 100 μm by 100 μm.

TLM Patterns

The TLM pattern contacts are 50μm by 100μm. See the section on TLM patterns for more details.

Van der Pauw Patterns

The VDP body is 100μm by 100μm. Each leg is 20μm wide with a single contact.

PMOS and NMOS Capacitor

The area for each capacitor is 400μm by 400μm.

NAND, NOR, and Inverter

All the transistors in the NAND, NOR, and Inverter have a channel length of 10 μm and a channel width of 65 μm.

Alignment Marks

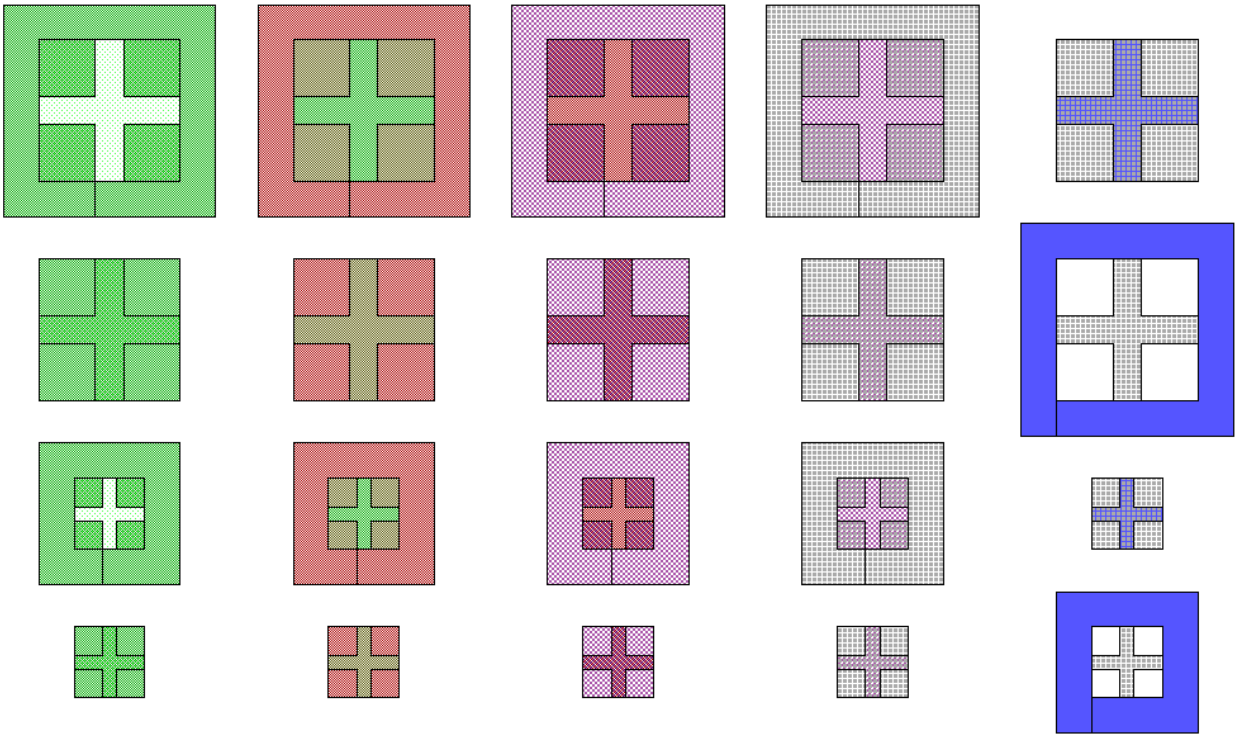


Figure 3: Alignment Marks

There are 4 different sets of alignment marks in the top right corner of each die. Half of these sets use a plus-sign type alignment, while the other half uses a square type alignment. The alignment begins with the p-well layer, either showing up as a plus or a square. This sets the initial alignment that the next mask will line up next to. The PMOS layer will then be lined up to the p-well layer, matching the square to the plus-sign, and the plus-sign to the square. This layer will also add a new plus-sign and square to be used to line up the next mask. This process goes on until the metal layer, where there will not be an extra mark at the end.

Figure 4: Alignment Marks Layer by Layer

NMOS Transistor Walkthrough

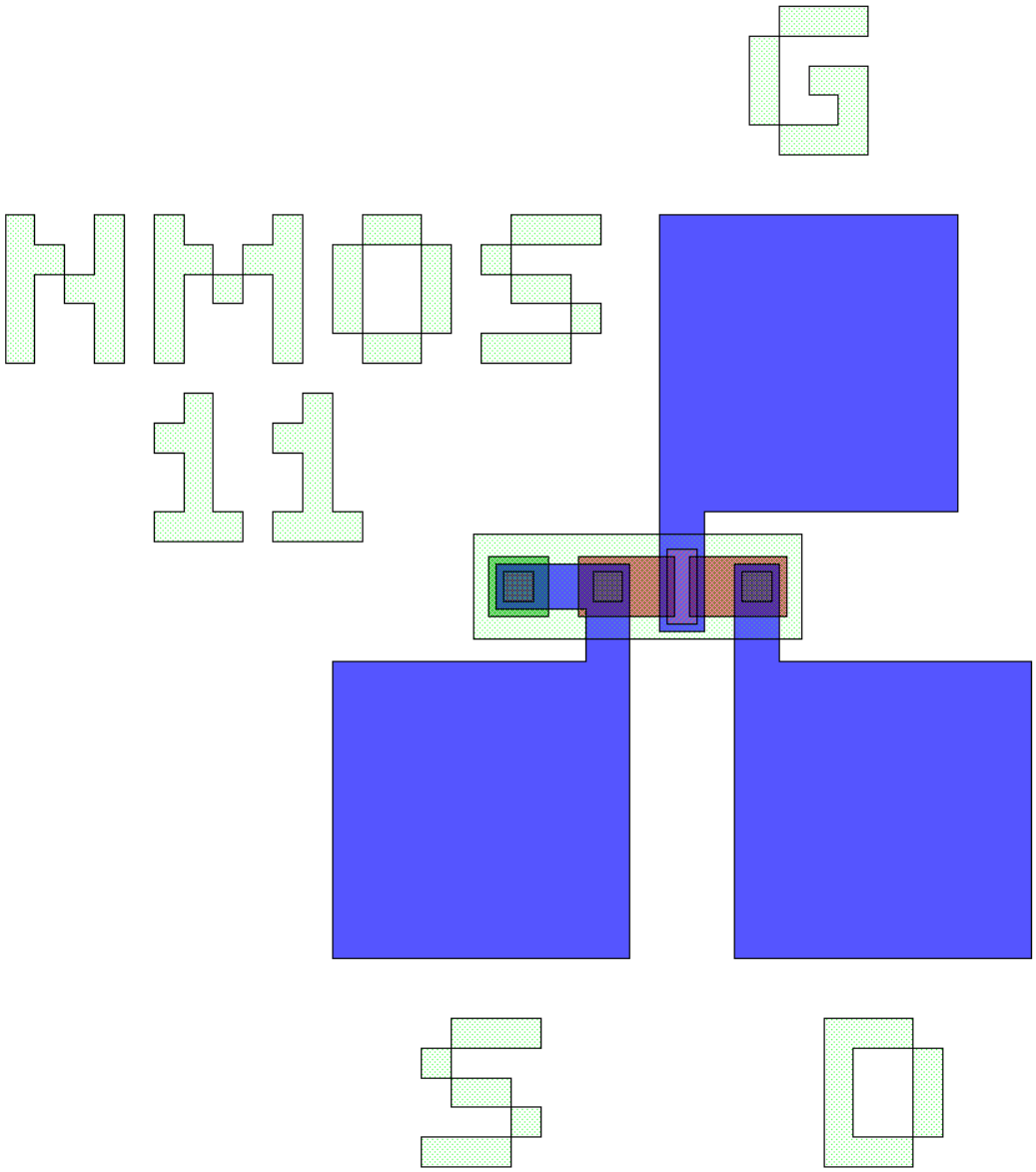


Figure 5: NMOS -- W=20 μm, L=5 μm

Mask 1 P-Well Diffusion

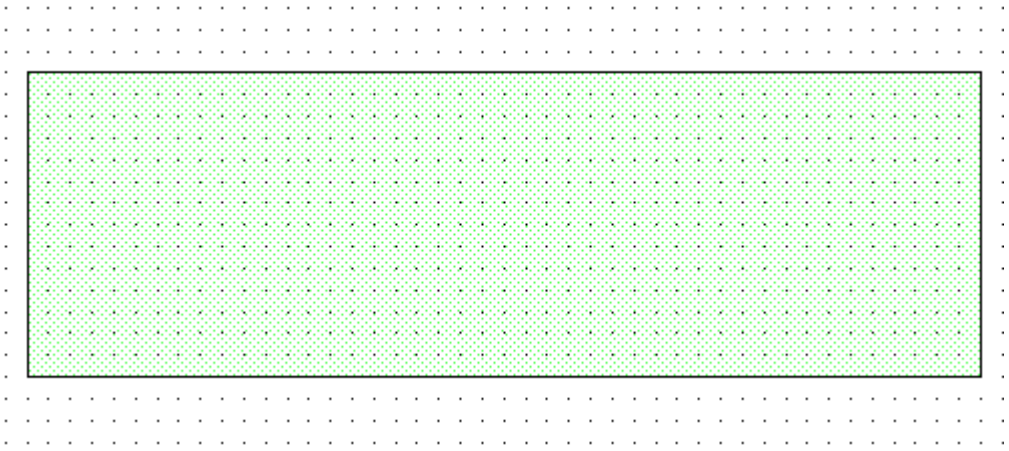


Figure 6: NMOS after P-Well

This layer adds the p-well layer to the wafer. This adds most of the lettering to the mask. The rest of the transistor will be built within this well.

Mask 2 PMOS Diffusion

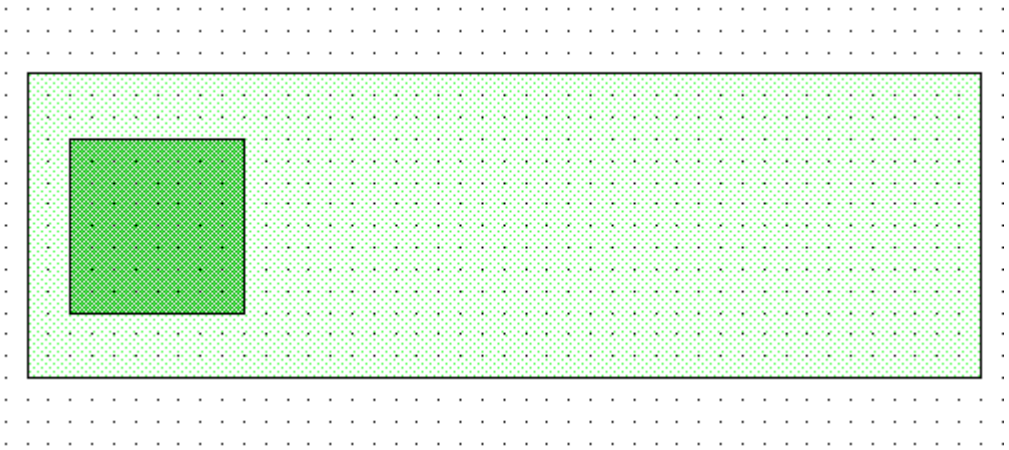


Figure 7: NMOS after PMOS diffusion

This creates a highly doped p-type region so contact can be made to the bulk of the transistor. In four terminal devices this is a separate contact. In a three terminal device this connects to the source of the transistor.

Mask 3 NMOS Source and Drain Diffusion

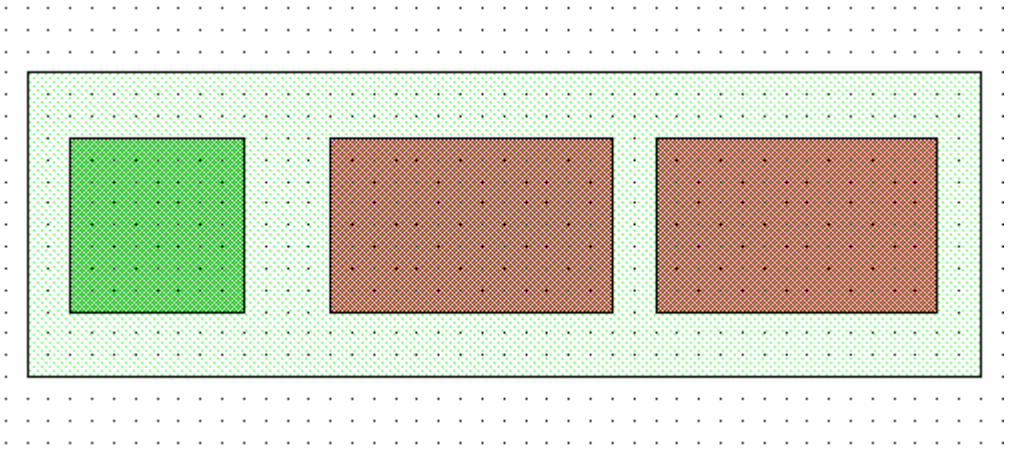


Figure 8: NMOS after NMOS diffusion

This creates a highly doped n-type region for the NMOS source and drain. The space between the source and drain is the channel. This space defines the W and L of the transistor.

Mask 4 Gate Oxide

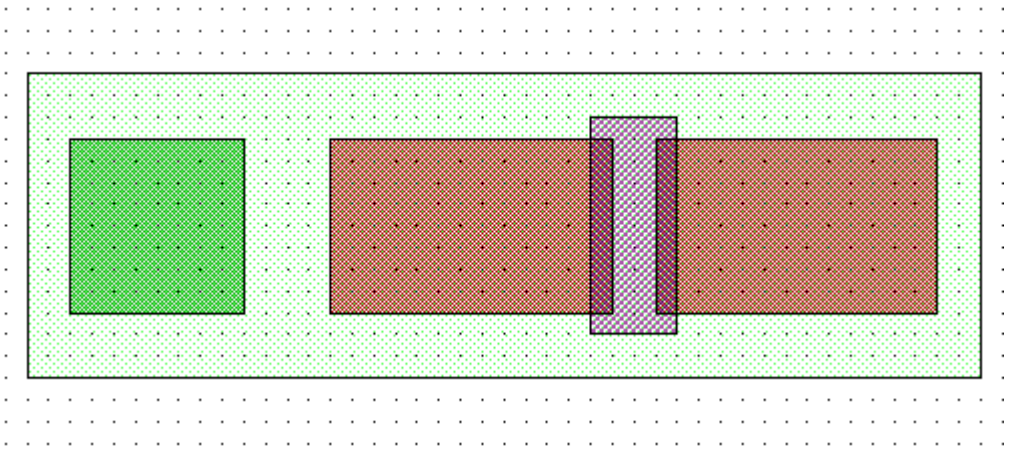


Figure 9: NMOS after gate oxide pattern

This patterns the area where a thin layer of oxide will be grown. It overlaps with the source and drain by $2.5\mu m$. This allows for a margin of error when aligning.

Mask 5 Contacts

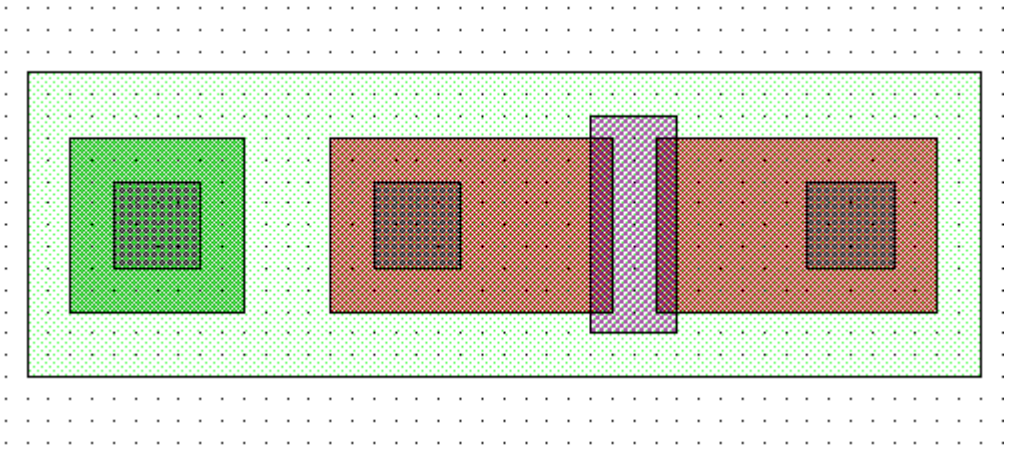


Figure 10: NMOS after contact patterning

The contact layer adds the contacts to the device, allowing the metal to connect to the device.

Mask 6 Metal

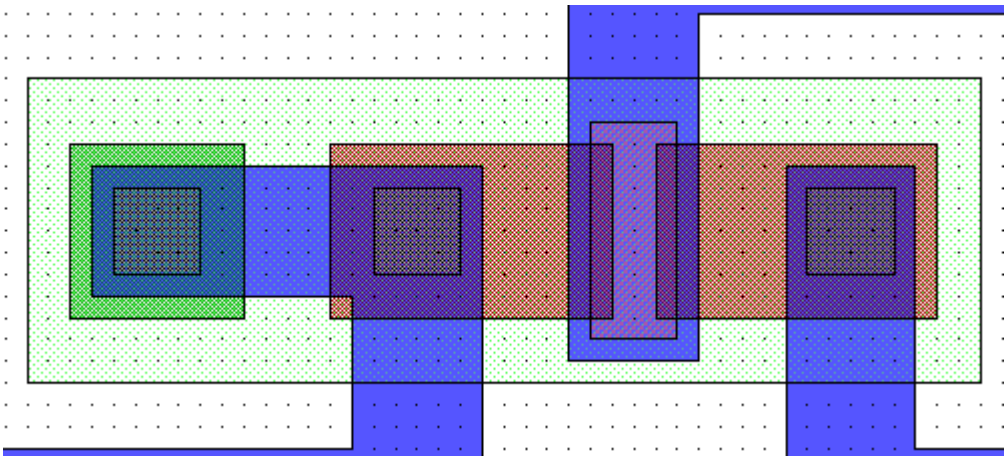


Figure 11: NMOS after metal

This layer is a light field mask. This means that most of the area will be transparent and where the metal will be patterned is opaque. The metal finishes connecting the devices, as well as gives an relatively large metal area for probes to test.

TLM Measurements

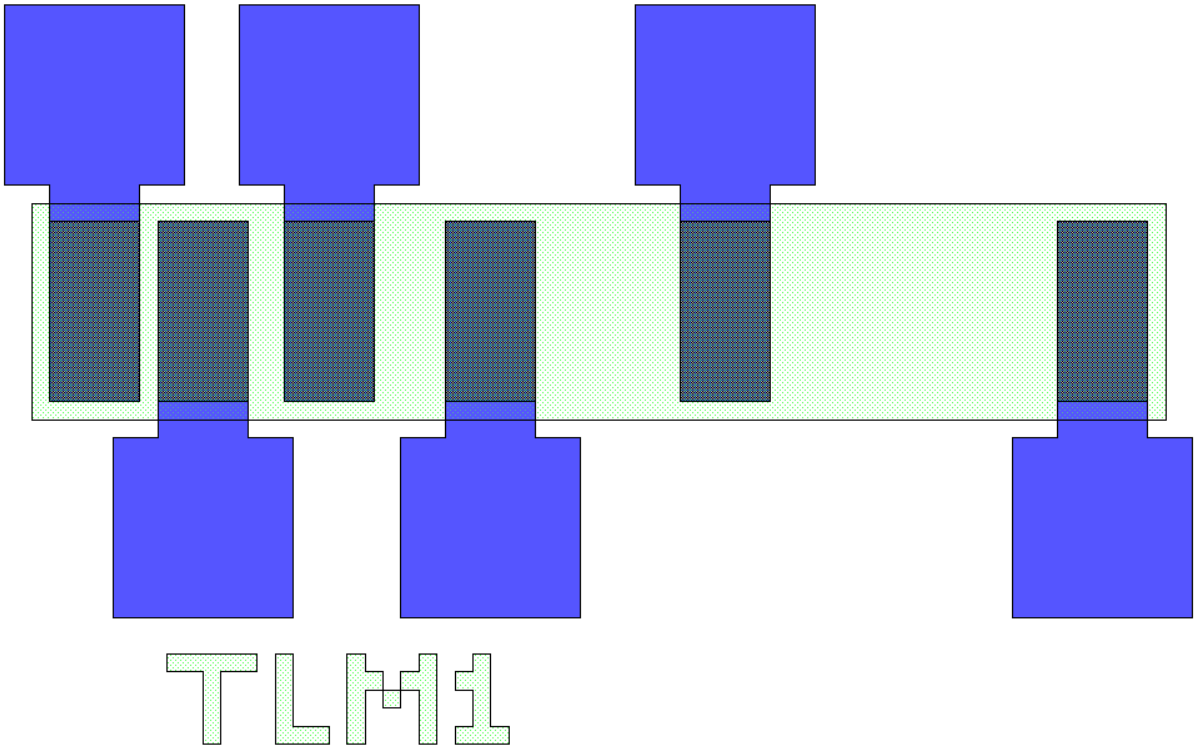


Figure 12: P-Well TLM

The TLM patterns in our dies are used to determine the resistance of the contacts, as well as the substrate. Each contact on the TLM pattern is spaced out twice as much as the last. To calculate the resistance, a voltage is applied and the current is measured. Dividing the current from the voltage gives the resistance. When you gather several of these measurements for different distances, you can create a resistance vs. distance graph. The slope of the line is the sheet resistance, and the y intercept is 2 times the contact resistance.

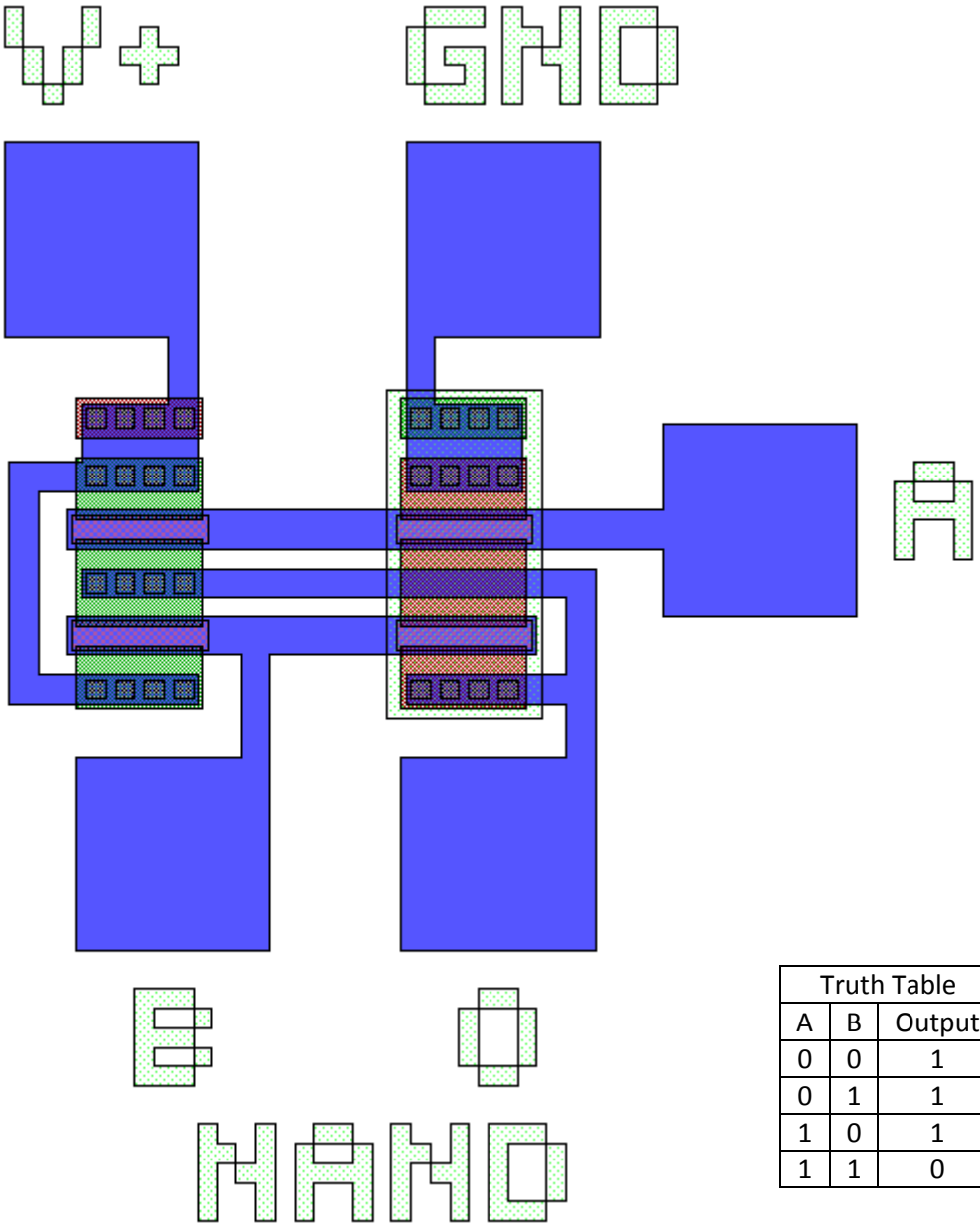
The distance between each of the contacts is shown in the table below.

D1	10 μm
D2	20 μm
D3	40 μm
D4	80 μm
D5	160 μm

The contact size is 50μm by 100μm. The height of the pattern is 120μm.

Additional Figures

NAND

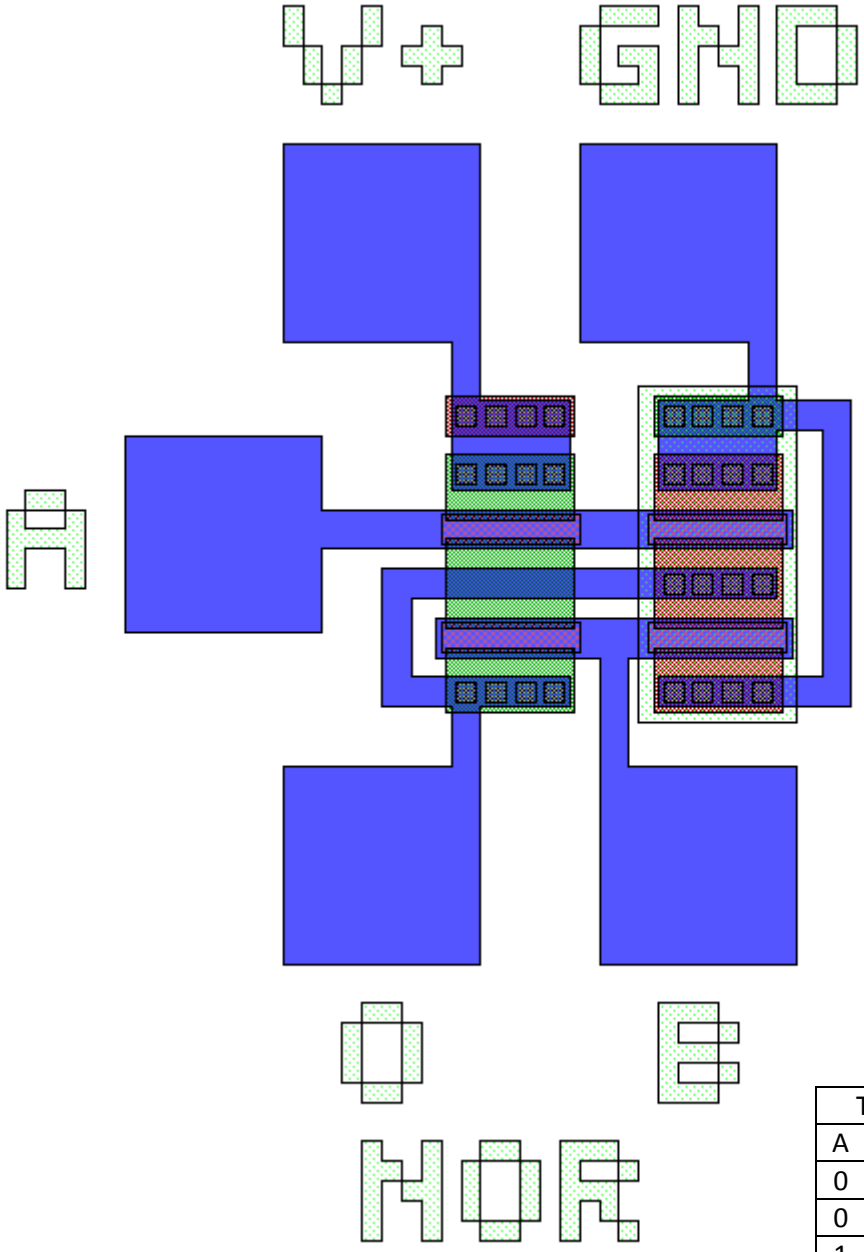


Truth Table		
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 13: NAND Gate

The gate is powered with V+ and GND. The inputs are A and B and the output is O. This gate implements the truth table above.

NOR

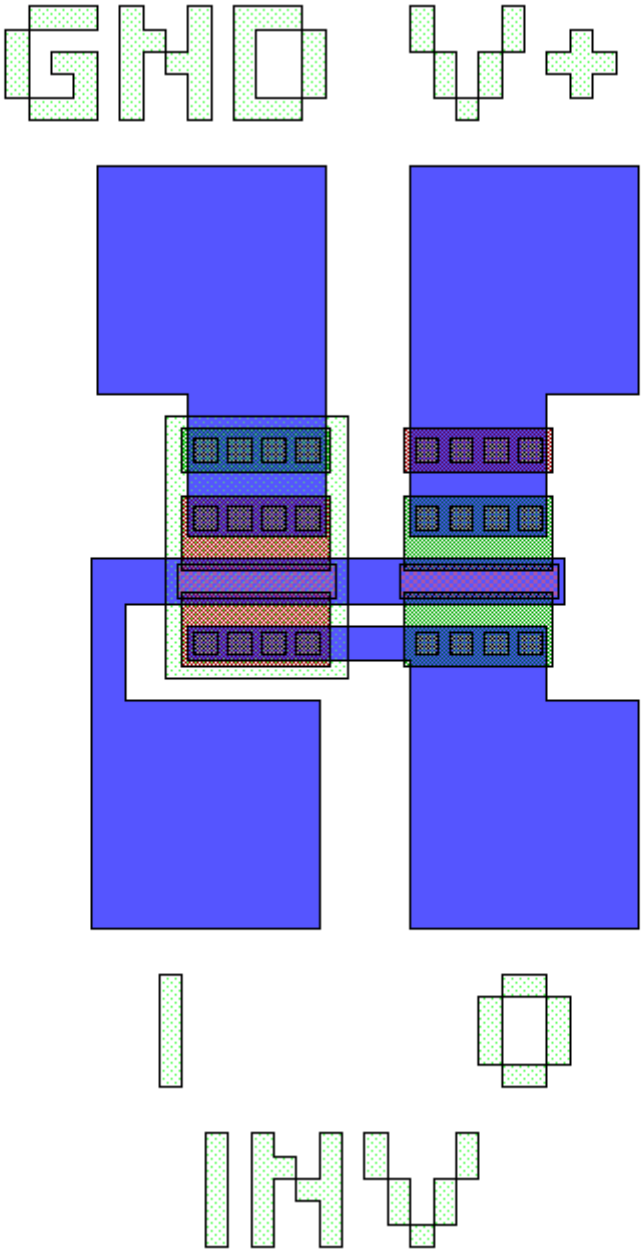


Truth Table		
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Figure 14: NOR Gate

The gate is powered with V+ and GND. The inputs are A and B and the output is O. This gate implements the truth table above.

Inverter



Truth Table	
I	Output
0	1
1	0

Figure 15: Inverter

The gate is powered with V+ and GND. The input is I and the output is O. This gate implements the truth table above.

BJT

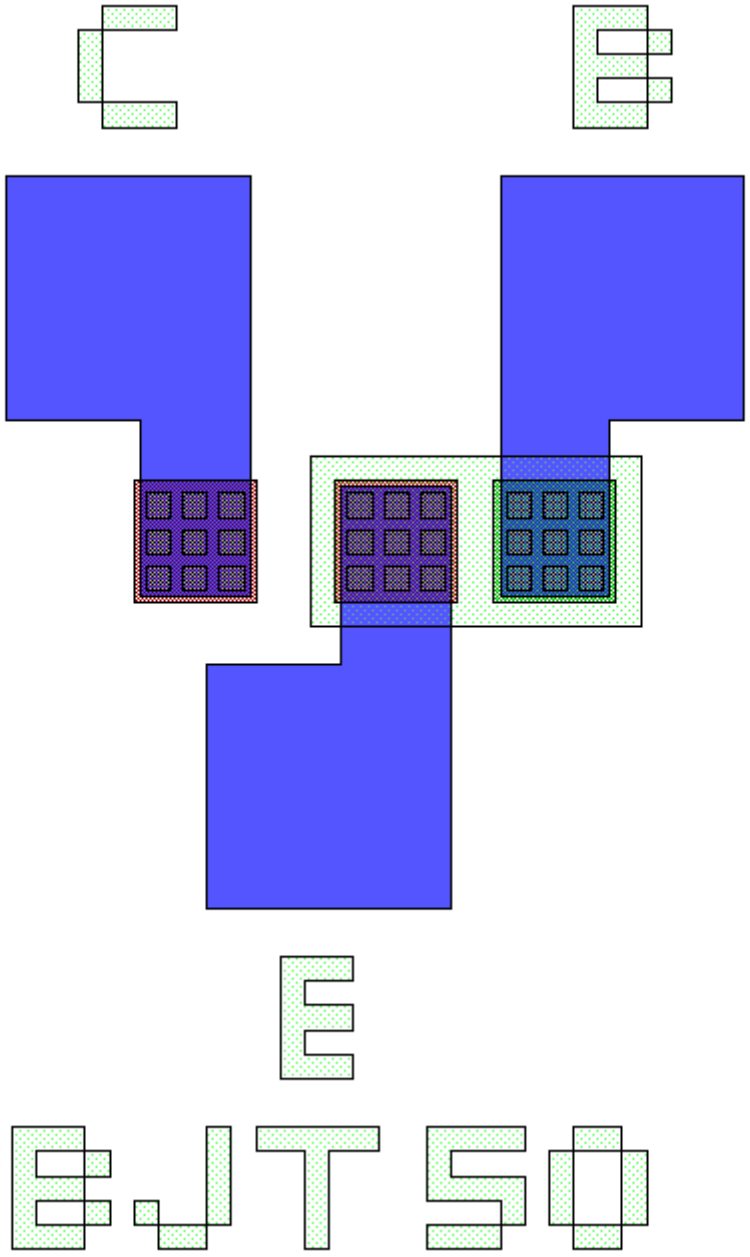


Figure 16: NPN BJT with A_e= 50μm by 50μm

This BJT is one of three NPNs on each die. This is the smallest version.