Real op amps (non-ideal aspects)

Things to consider

• power supplies and output voltage limits
• output current limitations
• finite gain
• finite $R_i$, non-zero $R_o$
• gain-bandwidth limits (seen previously)
• slew rate
• DC offsets
Power supplies and voltage limits

We know that op-amps need power supplies in order to function. The op-amp is really just a power converter, taking some of DC power from the supplies and converting it to signal power sent to output. The power supplies also impose limits on the output voltage – we can’t get out more than what goes in. When we try to exceed those limits, the output will “clip” at the limiting voltage.

The output limits depend on the particular op-amp. The limit of older chips, like the 741 or 324, will be 1 V – 2 V less than the power supply. And the limits may not be symmetric. For example, in using a 324 with ± 15 V supplies, the output may clip at 14 V on the positive side and -13.5 on the negative side. So be sure to check both high and low.

Some op-amps, like the LMC660 provide “rail-to-rail” outputs, meaning that the output can to with a few millivolts of the power-supply voltages. This can be advantageous in trying to maximize output power and in certain types of non-linear circuits. (More on this later.)
Ideal

Real

\[ V_{out} \]
\[ V_{in} \]
\[ G \]

\[ V_{out} \]
\[ V_{in} \]
\[ L_+ \]
\[ L_- \]
Also, some op-amps can work with a single power-supply. In that case, the negative side can be connected to ground. Using a single supply can be advantageous in battery powered applications. However, since the output voltage cannot go negative, the circuit must be designed to accommodate that limitation. (We will discuss single-supply designs in a future lecture.) Not all op-amps will work with a single supply. The 324 and 660 with both work with a single supply, but the 741 will not.

Be sure to check power supply limits in the data sheets, and do not exceed them in your application. For example, the 741 can have powers supplies up to \( \pm 20 \text{ V} \) (total difference of 40 V), the 324 can have a total power supply difference \( (V_{L+} - V_{L-}) \) of 32 V, and the 660 is limited to a total difference of just 16 V. There may also be a minimum power supply voltage needed in order for the amp to operate.

Lastly, in low-power applications a designer may need to worry about how much power is lost in the amp itself when there is no signal applied. This is known as quiescent power dissipation. Some amps are designed specifically for low-power dissipation.
Output current limits

Most general-purpose op amps have relatively modest output current capabilities. Internally, there is a simple circuit that purposely limits the amount of current that can flow through the output transistors. If too much current flows, the output transistors can be overheated and destroyed.

The current limit is usually set in the range of 30 mA - 80 mA for general purpose amps. This means that the amp cannot deliver very high power to a load.

For example, suppose you wanted to use a 741 op amp to try to drive a speaker, with has an 8-Ω coil (modeled as a load resistance of 8 Ω). If you wanted a 1-V amplitude on the output signal, the required output current would be as 125 mA. This is well beyond the 25-mA capability of the 741. The current would be limited and the signal would be distorted.

You would either have to add a special output stage between the 741 and the speaker (We’ll see how to do this later.) or use a special high-power op amp, like the venerable LM 383, which can output 3.5 A.
Finite gain

Of course, a real amp cannot have infinite gain. How much difference will a finite gain have on circuit performance? To see, consider and inverting op amp circuit. Replace the op amp with its two-port equivalent.

Since the gain is not infinite, we cannot employ the virtual short at the input, $v_1 \neq 0$

$$i_{R1} = i_{R2}$$
$$\frac{v_i + v_1}{R_1} = -\frac{v_1 - v_o}{R_2}$$
$$v_o = Av_1$$

$$v_i + \frac{v_o}{A} = \frac{-v_o}{A} - v_o$$

$$G = \frac{-\frac{R_2}{R_1}}{1 + \frac{1}{A} \left(1 + \frac{R_2}{R_1}\right)}$$

If $R_2/R_1 = 20$, then a 1% error in closed-loop gain ($G = -19.8$) would require that $A < 2000$. No op-amp is that bad.
Finite $R_i$

To see if having finite input resistance has an effect on the gain, we can look at the same inverting circuit, but include an input resistance along with the finite gain.

\[ i_{R1} = i_{R2} + i_{Ri} \]

\[ \frac{v_i + v_1}{R_1} = \frac{-v_1 - v_o}{R_2} + \frac{-v_1}{R_i} \]

\[ G = \frac{v_o}{v_i} = \frac{-\frac{R_2}{R_1}}{1 + \frac{1}{A} \left(1 + \frac{R_2}{R_1} + \frac{R_2}{R_i}\right)} \]

The $R_2/(A R_i)$ term in the denominator represents the effect of the input resistance. If $R_2 = 20 \text{ k}\Omega$, $R_i = 1 \text{ M}\Omega$, and $A = 10^4$, then that term is $2 \times 10^{-6}$, which is essentially negligible in most applications. Furthermore, the input resistance to the entire circuit (including the feedback elements) is simply $R_1$, if $R_i$ and $A$ are both relatively large.
Non-zero $R_o$

We can use the same trick to see the effect of non-zero output resistance.

This requires two node-voltage equations.

\[ i_{R1} = i_{R2} \]
\[ \frac{v_i + v_1}{R_1} = -\frac{v_1 - v_o}{R_2} \]
\[ i_{R2} = i_{R0} \]
\[ -\frac{v_1 - v_o}{R_2} = \frac{v_o - Av_1}{R_2} \]

With a bit of algebra to eliminate $v_1$, we arrive at the expression for the closed-loop gain with a non-zero $R_o$:

\[ G = \frac{v_o}{v_i} = \frac{-\frac{R_2}{R_1}}{1 + \left( \frac{R_2 + R_o}{AR_2 - R_o} \right) \left( 1 + \frac{R_2}{R_1} \right)} \]

With $R_2 = 20 \, \text{k}\Omega$, $R_1 = 1 \, \text{k}\Omega$, $R_o = 100 \, \Omega$, and $A = 10^4$, the closed-loop gain is -19.96. (Compared to $G = -20$ if $R_o = 0$.)
Gain-bandwidth

We have a separate set of notes on the bandwidth limitation of op amps. You should re-read those, since GBW is one of the most important properties of “real” op amps.

Slew rate

Another limitation is the “slew rate” of the op amp, meaning that there is a limit on how fast the output voltage can change. This is a hard limit and can be another source of distortion.

\[ SR = \left. \frac{dV_o}{dt} \right|_{\text{max}} \]

Whenever the output tries to change faster than this, the output rate-of-change will be limited to the slew rate.

Slew-rate limits can be most easily seen when an op amp circuit is amplifying a square wave – the output won’t keep up.
Although slew rate limits are most evident with square-wave transitions, they can affect any waveform. Consider a sinusoid at the output: \( v_o(t) = V_m \cos(\omega t) \).

The time rate of change for the cosine is
\[
\frac{dv_o}{dt} = -\omega V_m \sin(\omega t)
\]

If the magnitude of the derivative ever becomes bigger than the slew rate, the output will become distorted. To avoid this problem, we would have to observe the following requirement:

\[
\left. \frac{dv_o}{dt} \right|_{\text{max}} = \omega V_m < \text{SR}
\]

Meaning that you may need to limit either the frequency or the amplitude of the output to avoid distortion.
Even though the slew rate imposes a frequency limit for sinusoidal signals, it is fundamentally different than the gain-bandwidth. Slew rate limits will distort the signal. The bandwidth limitation will give an undistorted signal, but with a possibly reduced amplitude.

Example: An op amp has listed slew rate of 1 V/µs. In trying to amplify a sine wave with output amplitude of 3 V, what is the highest frequency that can be used without distortion?

\[
f < \frac{\text{SR}}{2\pi V_m} = \frac{1 \text{ V/µs}}{2\pi (3 \text{ V})} = 53 \text{ kHz}
\]
Offset voltage and bias current

The circuit at right is an inverting amp with no input voltage. (Or is it a non-inverting amp with no input?) Whichever, we expect the output voltage to exactly zero for an ideal op amp.

However, if we do this in lab, we would find a non-zero DC voltage at the output. This is the result of two more imperfections: DC offset voltages and bias currents. DC offset voltages result from imperfect matching of transistors at the input of the op amp. These are manufacturing imperfections and show up in all op amps. Bias currents are small DC currents needed for proper operation of the transistors at the inputs of some op amps. The current level varies widely for different op amps. It is rarely bigger than a few microamps (as for the 741 and 324) and can be nearly negligible for some amps (picoamp range for the 660).
The end effects of offset voltages and bias currents are the same: unexpected DC output voltages. For simplicity, we’ll start by considering the two separately.

**DC offset voltages**

We’re not yet able to understand the origin of offset voltages. However, the effect is easy to model: Simply add a DC voltage to the non-inverting input of an otherwise ideal op amp.

\[
\begin{align*}
\text{It looks like a non-inverting amp.}
\end{align*}
\]

\[
v_{oDC} = \left(1 + \frac{R_2}{R_1}\right) V_{OS}
\]

Since the error is associated with the input of the op amp, it will be multiplied by the gain of the circuit. Obviously, offset problems are worse for amps with high gain.
Example

An inverting amp is made using $R_2/R_1 = 500$. The input signal is $V_s = (10\text{mV})\sin\omega t$. The offset voltage for the op amp is 5 mV. What is the expected output voltage?

This could be analyzed using a several different methods. Here’s one approach.

\[
\frac{v_i - v_-}{R_1} = \frac{v_- - v_o}{R_2}
\]

\[
v_- = V_{OS}
\]

\[
v_o = -\frac{R_2}{R_1}v_i + \left(1 + \frac{R_2}{R_1}\right)V_{OS}
\]

\[
= -(5 \text{ V}) \sin \omega t + 2.5 \text{ V}
\]
Since voltage offset results from manufacturing variations, it will be a random variable — positive for one amp, negative for another, and maybe zero for a third. So the average over a large number of amps would be zero. However, this gives an improper view of the problem. Instead, we should average the magnitude of the offset. For most op amps, the average of the magnitude is on the order of a few millivolts.

It is possible to buy “high-precision” amps, that have smaller offset voltages, but you pay more than you would for general-purpose amps.
Some older op amps (ones using bipolar transistors) require a small amount of current inflow in order to work properly. Again, we can’t yet understand the details, but the effect is easy to model — add a pair of current sources at the inputs.
To see the effect of the bias current, hook up an inverting amp.

Using virtual ground: $V_- = V_+ = 0$.

Then: $v_{o\text{DC}} = I_{bias}R_2$

So this will be a problem whenever $R_2$ is large (as in the case of high-gain amps).
It is possible to cancel out the effects of the bias currents by shifting the non-inverting terminal from ground, i.e. having $v_+ \neq 0$. Put a resistor between ground and the non-inverting terminal.

\[
\frac{v_-}{R_1} + \frac{v_- - v_o}{R_2} + I_{bias} = 0
\]

\[
v_- = v_+ = -I_{bias}R_3
\]

\[
v_o = I_{bias} \left( R_2 - R_3 - \frac{R_2R_3}{R_1} \right)
\]

The output will be zero, if we choose $R_3 = R_1||R_2$
Although we’ve treated them separately, offset voltage and bias currents will occur together and we can’t necessarily sort them out.

Use superposition (or solve node voltages from scratch, as done below) to see the cumulative effect.

\[
\frac{v_-}{R_1} + \frac{v_- - v_o}{R_2} + I_{bias} = 0 \quad v_- = v_+ = -I_{bias}R_2 + V_{os}
\]

\[
v_o = \left( R_2 - R_3 - \frac{R_2R_3}{R_1} \right) I_{bias} + \left( 1 + \frac{R_2}{R_1} \right) V_{os}
\]

If \( R_3 = R_1 \parallel R_2 \) then \( v_o = \left( 1 + \frac{R_2}{R_1} \right) V_{os} \) We see offset voltage effect only.
Example (like lab)

Set up the inverting circuit with $R_2/R_1 = 680\text{k}\Omega/1\text{k}\Omega$ with no input and set $R_3 = R_1||R_2$. The bias current effect should be zeroed out. If we then measure the output voltage to be -2.0 V, we can calculate $V_{OS}$.

$$V_{OS} = -2.0\text{V}/681 = -2.9 \text{ mV}.$$ 

Then remove $R_3$ (i.e. make it zero) and measure the output to -0.5 V. Since the bias currents aren’t canceled in this case,

$$v_o = R_2 I_{bias} + \left(1 + \frac{R_2}{R_1}\right)V_{os}$$

$$I_{bias} = \frac{v_o - \left(1 + \frac{R_2}{R_1}\right)V_{os}}{R_2}$$

$$= \frac{-0.5 \text{ V} - (-2.0 \text{ V})}{680 \text{ k}\Omega} = 2.2 \mu\text{A}$$
Note that $V_{OS}$ can be positive or negative, and the bias currents can also be positive or negative, depending on the type of transistors at the input.

A further complication is that the bias currents may be mismatched also, for much the same reason that there is an offset voltage. So we could take the analysis one step further and include current differences. However, these effects are usually very small and not worth extra effort here.

Modern op amps (using CMOS technology) have exceptionally tiny bias currents — so small that we probably don’t even need to consider them.

Offset voltages and bias currents are particularly problematic in high-gain amps and integrating circuits.

Some op amps have extra connections that can be used to try to cancel offset voltages (eg. 741). Read the data sheet to see how to use these. We can also use summing amp techniques to try cancel offsets.