TAKE THE HOLES

AND PUSH THEM SOMEWHERE ELSE
4-terminal

3-terminal — body tied to source

digital

power

NMOS examples
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\[ K_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \]
For the circuit shown, use the NMOS equations to find $i_D$ and $v_{DS}$.

For the NMOS, $V_T = 1.5 \, V$ and $K = 0.5 \, mA/V^2$.

$v_{GS} = V_G = 4 \, V \rightarrow$ the NMOS is on.

Assume that the transistor is in saturation.

\[ i_D = K (v_{GS} - V_T)^2 = \left(0.5 \, mA/V^2\right) [4V - 1.5V]^2 = 3.125 \, mA \]

\[ v_{DS} = V_{DD} - i_D R_D = 10V - (3.125 \, mA) (2k\Omega) = 3.75V \]

\[ v_{GS} - V_T = 4 \, V - 1.5 \, V = 2.5 \, V \]

\[ v_{DS} > v_{GS} - V_T \rightarrow \text{saturation confirmed. Q.E.D.} \]
Example 2

For the circuit shown, use the the NMOS equations to find $i_D$ and $v_{DS}$.

For the NMOS, $V_T = 1.0\ V$ and $K = 0.5\ \text{mA/V}^2$.

Since $V_G > V_T \rightarrow$ the NMOS is on.

Guess that the transistor is in saturation.

\[ i_D = K(v_{GS} - V_T)^2 \]

\[ v_{GS} = V_G - i_S R_S \] (and $i_S = i_D$, as always for a FET)

\[ i_D = K(V_G - i_D R_S - V_T)^2 \]

\[ = K \left[ R_S^2 i_D^2 - 2(V_G - V_T) R_S i_D + (V_G - V_T)^2 \right] \]

Re-arranging:

\[ i_D^2 - \left[ \frac{1}{KR_S^2} + 2 \left( \frac{V_G - V_T}{R_S} \right) \right] i_D + \left[ \frac{V_G - V_T}{R_S} \right]^2 = 0 \]
\[ i_D^2 - \left( \frac{1}{KR_S^2} + 2 \left( \frac{V_G - V_T}{R_S} \right) \right) i_D + \left( \frac{V_G - V_T}{R_S} \right)^2 = 0 \]

Plug in the numbers:

\[ i_D^2 - [10 \text{ mA}] i_D + [16 \text{ mA}^2] = 0 \]

Use the quadratic equation:

\[ x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \]

or, if \( a = 1 \)

\[ x = -\frac{b}{2} \pm \sqrt{\left(\frac{b}{2}\right)^2 - c} \]

Which one is correct? Check \( v_{GS} \) for both.

If \( i_D = 8 \text{ mA} \), \( v_{GS} = V_G - i_DR_S = 5 \text{ V} - 8 \text{ V} = -3 \text{ V} \). No way! If \( v_{GS} = -3 \text{ V} \), the NMOS would not even be on.

For \( i_D = 2 \text{ mA} \), \( v_{GS} = V_G - i_DR_S = 5 \text{ V} - 2 \text{ V} = 3 \text{ V} \). This is OK.

Finally, \( v_{GS} - V_T = V_G - i_DR_S - V_T = 2 \text{ V} \), and \( v_{DS} = V_{DD} - i_DR_D - i_DR_S = 4 \text{ V} \).

\( v_{DS} > v_{GS} - V_T \rightarrow \) saturation confirmed.
Example 3

For the circuit shown, use the NMOS equations to find $i_D$ and $v_{DS}$.

For the NMOS, $V_T = 1.5 \, \text{V}$ and $K = 0.25 \, \text{mA/V}^2$.

First note that $v_{GS} = v_{DS}$, so the NMOS must be in saturation. ($v_{DS} > v_{GS} - V_T$) No guess needed.

Since $V_{DD} > V_T \rightarrow$ the NMOS is on.

And $i_S = i_D$ (always for a FET) and don’t forget that $i_G = 0$.

\[
i_D = K (v_{GS} - V_T)^2 \quad v_{GS} = V_{DD} - i_S R_S
\]

\[
i_D = K (V_{DD} - i_D R_S - V_T)^2
\]

\[
= K \left[ R_S^2 i_D^2 - 2 (V_{DD} - V_T) R_S i_D + (V_{DD} - V_T)^2 \right]
\]

(Same basic form as Example 2.)

\[
i_D^2 \left[ \frac{1}{K R_S^2} + 2 \left( \frac{V_{DD} - V_T}{R_S} \right) \right] i_D + \left[ \frac{V_{DD} - V_T}{R_S} \right]^2 = 0
\]
\[ i_D^2 - \left[ \frac{1}{KR_S^2} + 2 \left( \frac{V_{DD} - V_T}{R_S} \right) \right] i_D + \left[ \frac{V_{DD} - V_T}{R_S} \right]^2 = 0 \]

Plug in the numbers:

\[ i_D^2 - [6.74 \text{ mA}] i_D + \left[ 8.73 \text{ mA}^2 \right] = 0 \]

Use the quadratic equation:

\[ i_D = 4.99 \text{ mA} \text{ or } i_D = 1.75 \text{ mA}. \]

Which is right? Check the \( v_{GS} \) for both.

If \( i_D = 4.99 \text{ mA} \), \( v_{GS} = V_{DD} - i_D R_S = 8 \text{ V} - 10.98 \text{ V} = -2.98 \text{ V} \).  Nope – the NMOS would not be on in the case.  This root is bogus.

If \( i_D = 1.75 \text{ mA} \), \( v_{GS} = V_{DD} - i_D R_S = 8 \text{ V} - 3.85 \text{ V} = 4.15 \text{ V} \).  OK, this works.

Finally, \( v_{DS} = v_{GS} = 4.15 \text{ V} \).
Example 4

For the circuit shown, use the NMOS equations to find $i_D$ and $v_{DS}$.

For the NMOS, $V_T = 1.5$ V and $K = 0.5$ mA/V$^2$.

$v_{GS} = V_G = 10$ V → the NMOS is on.

This looks like a lot like the first example. So start by assuming that the NMOS is in saturation.

\[
\begin{align*}
    i_D &= K (v_{GS} - V_T)^2 = \left(0.5 \text{ mA}/\text{V}^2\right)[10\text{ V} - 1.5\text{ V}]^2 = 36.125\text{ mA} \\
    v_{DS} &= V_{DD} - i_D R_D = 10\text{ V} - (36.125\text{ mA}) (2\text{ k}\Omega) = -62.25\text{ V}
\end{align*}
\]

Red Alert! There is a serious problem here. Apparently the NMOS is not in saturation. So try the ohmic equation.

\[
    i_D = K [2 (v_{GS} - V_T) v_{DS} - v_{DS}^2]
\]

Unfortunately, we don’t know either $i_D$ or $v_{DS}$. So we need a second equation.
\[ i_D = K \left[ 2 (v_{GS} - V_T) v_{DS} - v_{DS}^2 \right] \]

Use Ohm’s law on the drain resistor to get a second equation:

\[ i_{RD} = \frac{V_{DD} - v_{DS}}{R_D} = i_D \]

We can use these to solve for either \( i_D \) or \( v_{DS} \). Setting the two equal and solving for \( v_{DS} \) is probably slightly easier.

\[ \frac{V_{DD} - v_{DS}}{R_D} = K \left[ 2 (v_{GS} - V_T) v_{DS} - v_{DS}^2 \right] \]

Re-arrange:

\[ v_{DS}^2 - \left[ 2 (v_{GS} - V_T) + \frac{1}{KR_D} \right] v_{DS} + \frac{V_{DD}}{KR_D} = 0 \]

Plug in numbers:

\[ v_{DS}^2 - [18 \text{ V}] v_{DS} + 10 \text{ V}^2 = 0 \]

Solve:

\[ v_{DS} = 0.574 \text{ V} \text{ or } v_{DS} = 17.43 \text{ V}. \]

It should be obvious that the larger value is way too big – it’s bigger than \( V_{DD} \). Also, since the NMOS is in ohmic, we expect \( v_{DS} \) to be small. So we choose the smaller value as correct.

Lastly:

\[ i_D = \frac{V_{DD} - v_{DS}}{R_D} = \frac{10 \text{ V} - 0.573 \text{ V}}{2\text{k} \Omega} = 4.71 \text{ mA} \]
Example 5

For the circuit shown, use the the NMOS equations to find \(i_D\) and \(v_{DS}\).

For the NMOS, \(V_T = 1\) V and \(K = 0.25\) mA/V\(^2\).

First note that since \(i_G = 0\), \(R_1\) and \(R_2\) form a simple voltage divider, and

\[
V_G = \frac{R_2}{R_2 + R_1} V_{DD} = 4\ \text{V}
\]

Since \(V_G > V_T\), the NMOS should be on. Guess that it is in saturation.

\[
v_{GS} = V_G - v_{RS} = V_G - i_D R_S
\]

\[
i_D = K (v_{GS} - V_T)^2 = K (V_G - i_D R_S - V_T)^2
\]

This is exactly the same as example 2.

\[
i_D^2 - \left[ \frac{1}{KR_S^2} + 2 \left( \frac{V_G - V_T}{R_S} \right) \right] i_D + \left[ \frac{V_G - V_T}{R_S} \right]^2 = 0
\]
\[ i_D^2 - \left[ \frac{1}{KR_S^2} + 2 \left( \frac{V_G - V_T}{R_S} \right) \right] i_D + \left[ \frac{V_G - V_T}{R_S} \right]^2 = 0 \]

Plug in the numbers:

\[ i_D^2 - [10 \text{ mA}] i_D + 9 \text{ mA}^2 = 0 \]

Use the quadratic equation:

\[ i_D = 9 \text{ mA} \text{ or } i_D = 1 \text{ mA}. \]

Which is right? Check the \( v_{GS} \) for both.

If \( i_D = 9 \text{ mA} \), \( v_{GS} = V_G - i_D R_S = 4 \text{ V} - 8.24 \text{ V} = -5 \text{ V} \), and

if \( i_D = 1 \text{ mA} \), \( v_{GS} = V_G - i_D R_S = 4 \text{ V} - 1 \text{ V} = 3 \text{ V} \).

Clearly, \( i_D = 1 \text{ mA} \) is the only answer that makes sense.

Finally, \( v_{GS} - V_T = 2 \text{ V} \), and \( v_{DS} = V_{DD} - i_D R_D - i_D R_S = 4.8 \text{ V} \).

\( v_{DS} > v_{GS} - V_T \rightarrow \text{saturation confirmed.} \)
Example 6

Same as example 5, but values for $R_2$ is increased to 680 kΩ. It is the same NMOS: $V_T = 1$ V and $K = 0.25$ mA/V².

Following the same procedure as Example 5, we obtain $V_G = 6.55$ V. Guessing saturation and performing the same calculation to find $i_D$,

$$i_D = 2.44 \text{ mA} \text{ or } i_D = 12.7 \text{ mA}.$$  

Again, the larger of these is clearly too big to make any sense. Checking the smaller value for consistency with saturation:

$$v_{GS} - V_T = V_G - i_D R_S - V_T = 3.11 \text{ V},$$  

$$v_{DS} = V_{DD} - i_D R_D - i_D R_S = 0.19 \text{ V}.$$  

Oops!! $v_{DS} < v_{GS} - V_T \rightarrow$ This is not in saturation!
So start over, assuming ohmic operation:

\[ i_D = K [2 (v_{GS} - V_T) v_{DS} - v_{DS}^2] \]

\[ v_{GS} - V_T = V_G - i_DR_S - V_T \]

\[ v_{DS} = V_{DD} - i_D R_D - i_D R_S \]

This is gonna be messy…

\[ \frac{i_D}{K} = 2 [V_G - i_D R_S - V_T] [V_{DD} - i_D (R_D + R_S)] - [V_{DD} - i_D (R_D + R_S)]^2 \]

After a whole lotta algebra…

\[ i_D^2 - \left[ \frac{1}{K (R_S^2 - R_D^2)} + \frac{2 R_S V_{DD}}{(R_S^2 - R_D^2)} + \frac{2 (V_G - V_T)}{(R_S - R_D)} - \frac{2 V_{DD}}{(R_S - R_D)} \right] i_D \]

(Ouch! That one hurt…)

\[ + \left[ \frac{2 (V_G - V_T) V_{DD} - V_{DD}^2}{(R_S^2 - R_D^2)} \right] = 0 \]

Plug in the numbers: \[ i_D^2 + [1.12 \text{ mA}] i_D - 6.45 \text{ mA}^2 = 0 \]

and the two roots are: \[ i_D = 2.04 \text{ mA} \] and \[ i_D = -3.16 \text{ mA} \].

Definitely ohmic.

\[ v_{DS} = 8 \text{ V} - (2.04 \text{ mA})(2.2 \text{ k}\Omega + 1 \text{ k}\Omega) = 1.47 \text{ V} \]
Example 7

Design the circuit at right (by choosing \( K \) for the NMOS and the value of \( R_S \)) so that \( i_D = 1 \text{ mA} \) and \( v_{DS} = 2.5 \text{ V} \). The NMOS has \( V_T = 1 \text{ V} \).

By writing a loop equation around the drain-source loop, we see that \( v_{RS} = V_{DD} - v_{DS} = 2.5 \text{ V} \). And so \( R_S = 2.5 \text{ V} / 1 \text{ mA} = 2.5 \text{ k}\Omega \).

Now writing a loop equation around the gate-source loop, we see that \( v_{GS} = V_G - v_{RS} = 1.5 \text{ V} \). This value of \( v_{GS} \) means that the NMOS must be operating in saturation.

Then, since in saturation \( i_D = K(v_{GS} - V_T)^2 \),

\[
K = \frac{i_D}{(v_{GS} - V_T)^2} = \frac{1 \text{ mA}}{(1.5 \text{ V} - 1 \text{ V})^2} = \frac{4 \text{ mA}}{V^2}
\]
Example 8

Design the circuit at right (by choosing $K$ for the NMOS and the value of $R_D$) so that $i_D = 10$ mA and $v_{DS} = 0.2$ V. The NMOS has $V_T = 1$ V. How much power is being dissipated in the resistor and the NMOS?

If $v_{DS} = 0.2$ V, then $v_{RD} = 9.8$ V. For a current of 10 mA, $R_D = v_{RD} / i_D = 9.8$ V / 10 mA = 0.98 kΩ.

With $v_{GS} = 5$ V and $v_{DS} = 0.2$ V, the NMOS must be working in the ohmic region. For ohmic operation:

$$i_D = K \left[ 2 (v_{GS} - V_T) v_{DS} - v_{DS}^2 \right]$$

$$K = \frac{i_D}{2 (v_{GS} - V_T) v_{DS} - v_{DS}^2} = \frac{10 \text{ mA}}{2 (5 \text{ V} - 1 \text{ V}) (0.2 \text{ V}) - (0.2 \text{ V})^2} = 6.41 \frac{\text{mA}}{\text{V}^2}$$

$$P_{RD} = (9.8 \text{ V}) (10 \text{ mA}) = 98 \text{ mW} \quad P_{NMOS} = (0.2 \text{ V}) (10 \text{ mA}) = 2 \text{ mW}$$