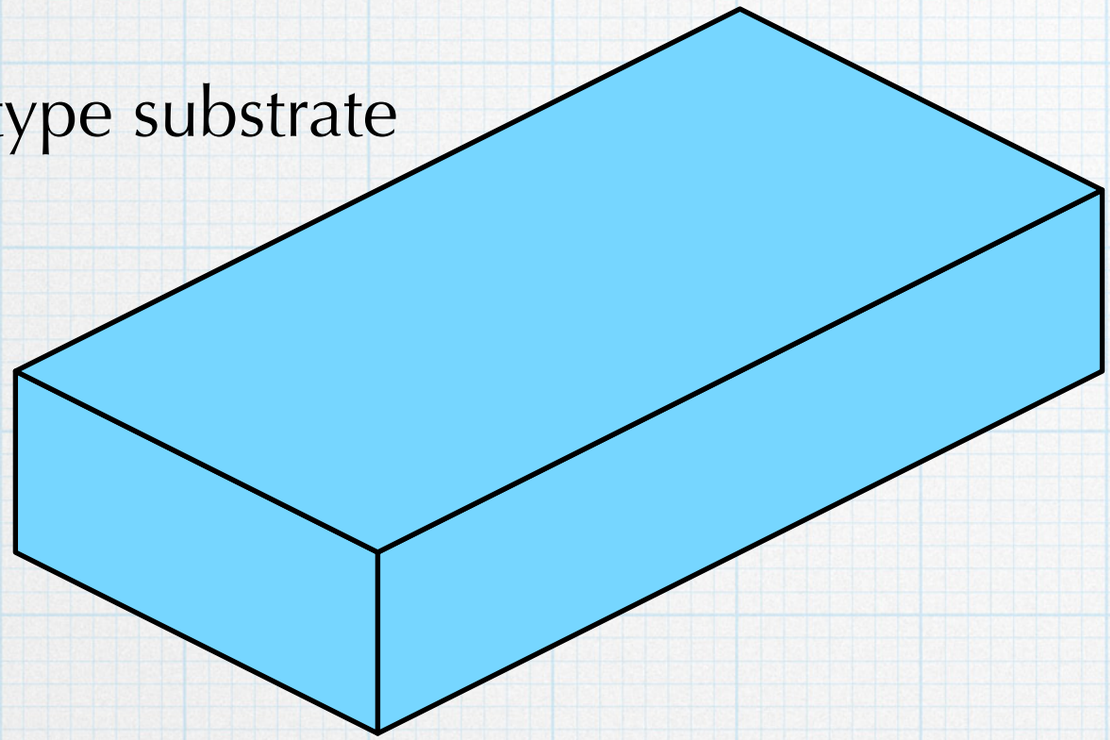
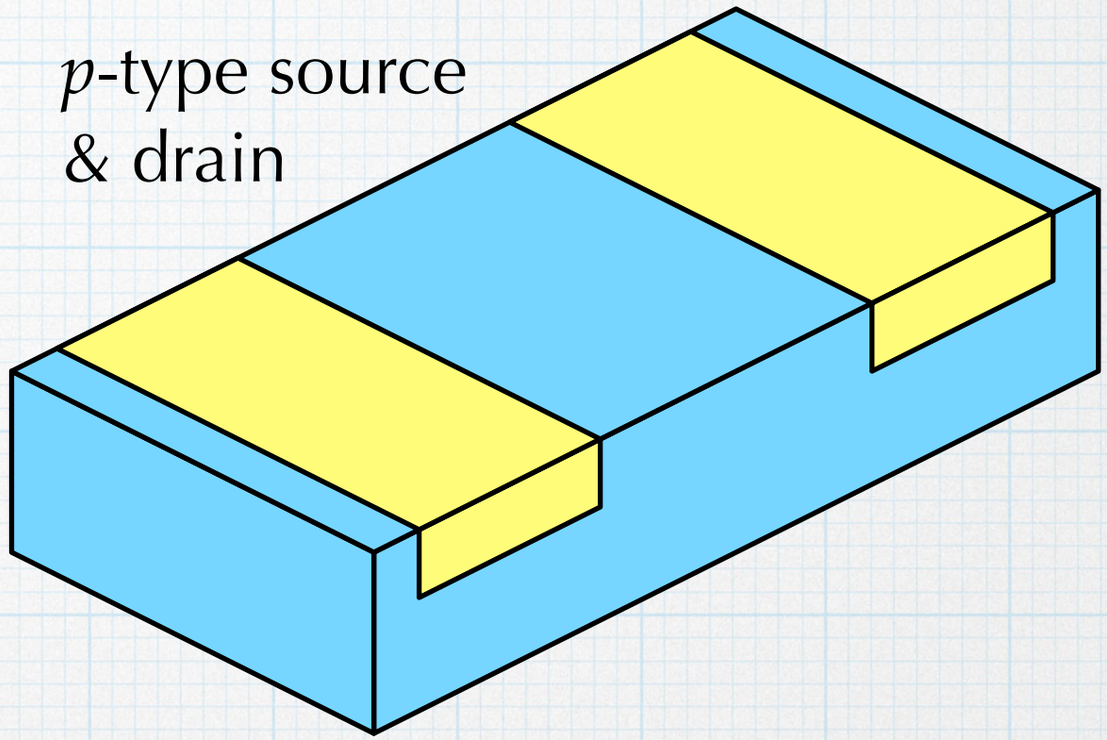
Basic PMOS structure

p-channel device (*n*- and *p*-type regions reversed.)

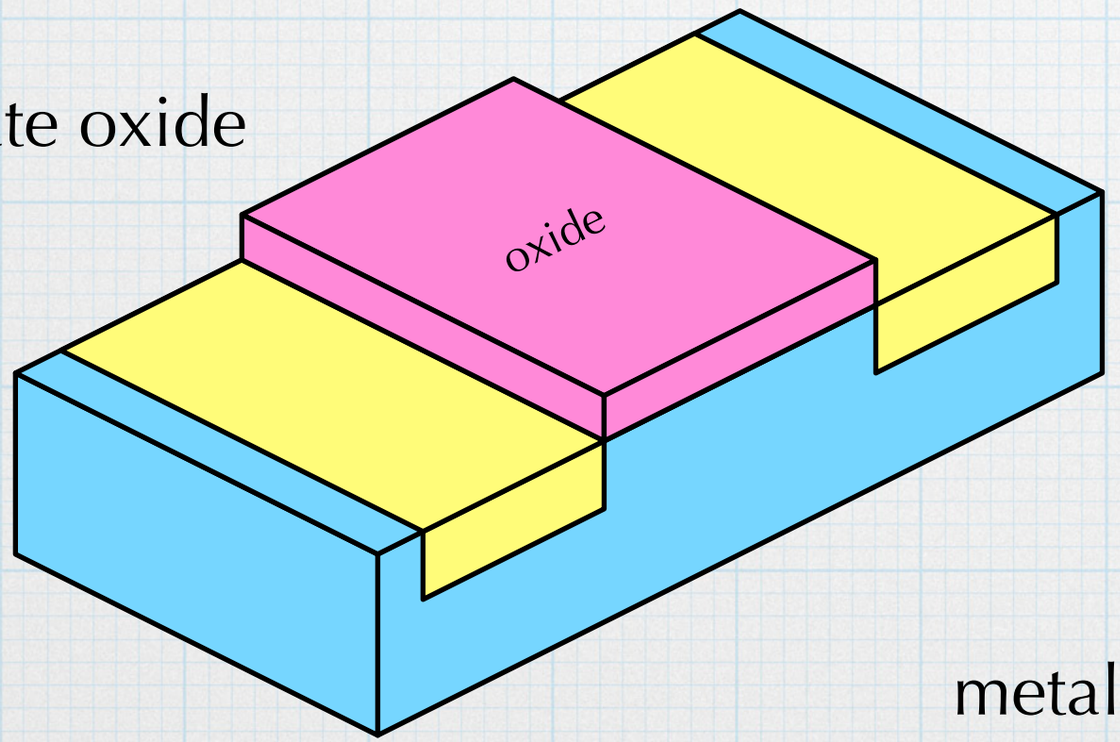
n-type substrate

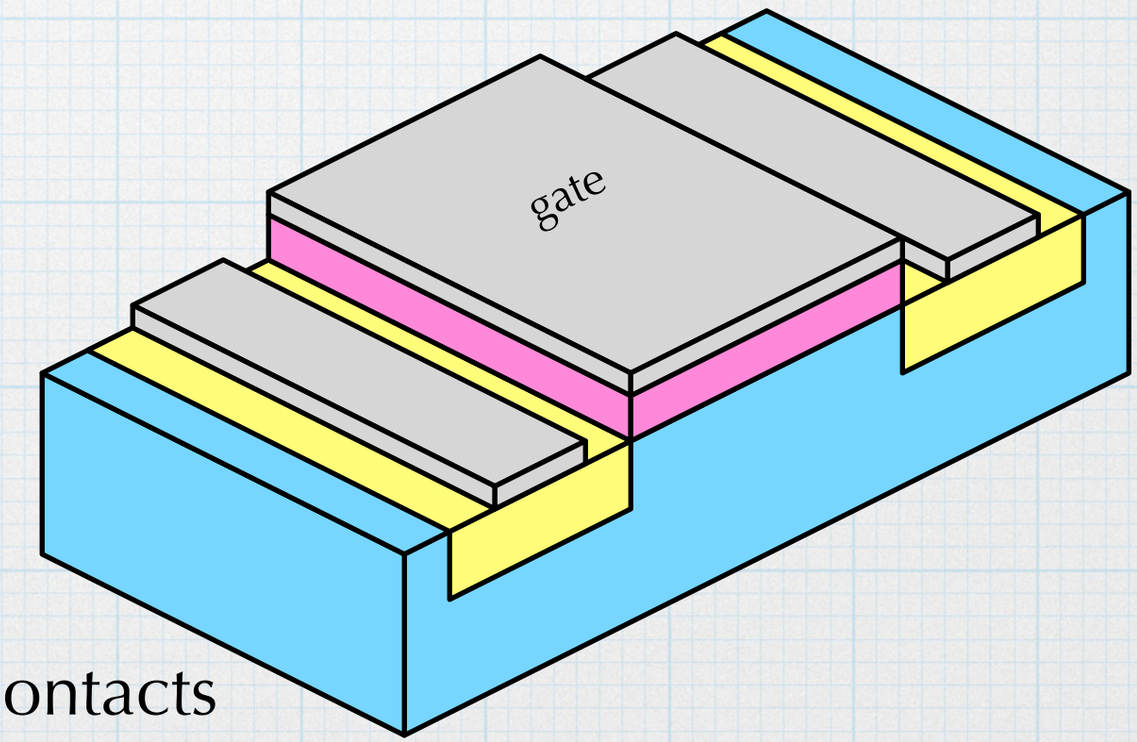


p-type source
& drain



gate oxide

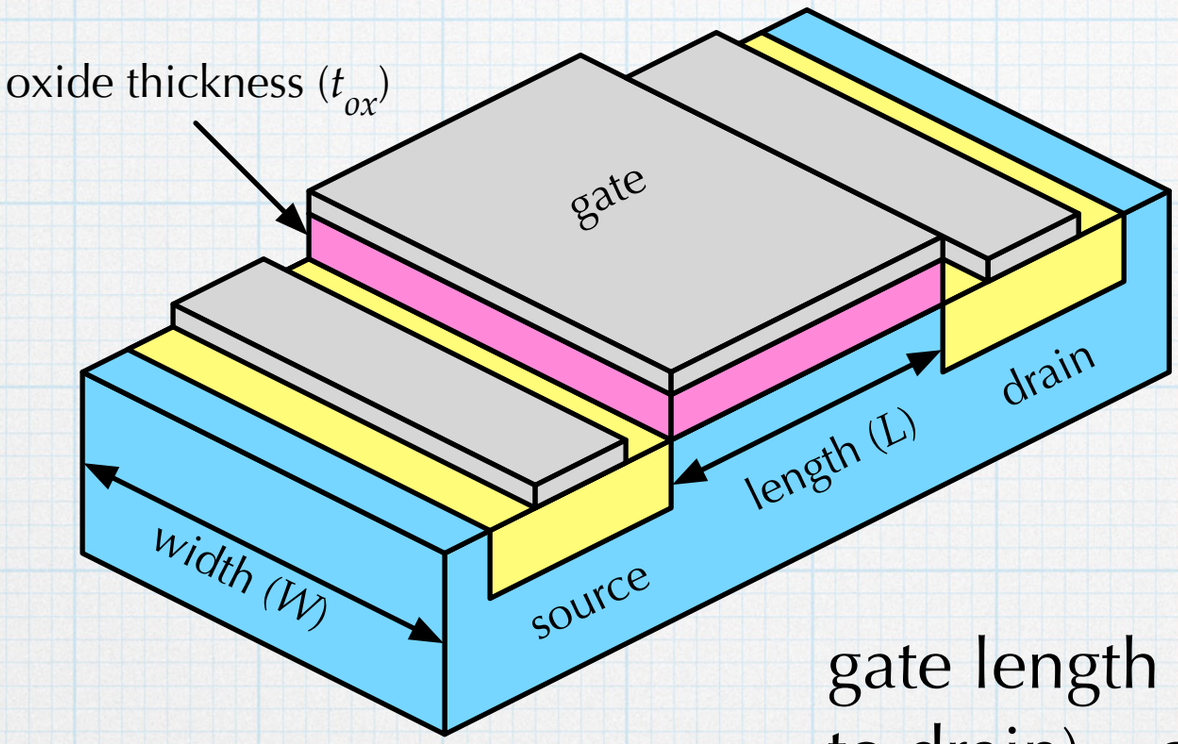




metal contacts

Critical dimensions

oxide thickness: typical 1 - 10 nm.

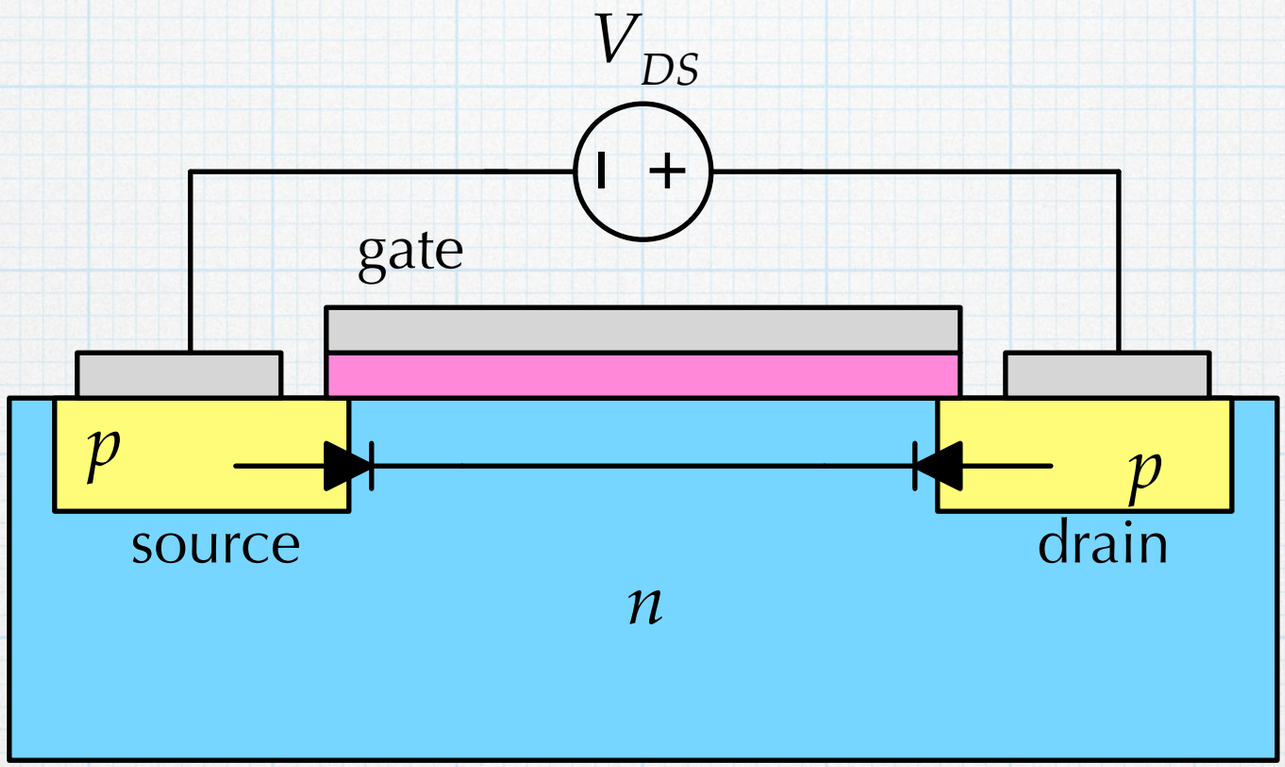


gate length (distance from source to drain) – currently as small as 20 nm.

width: typical L to 10 L (W/L ratio is important)

Will current flow?

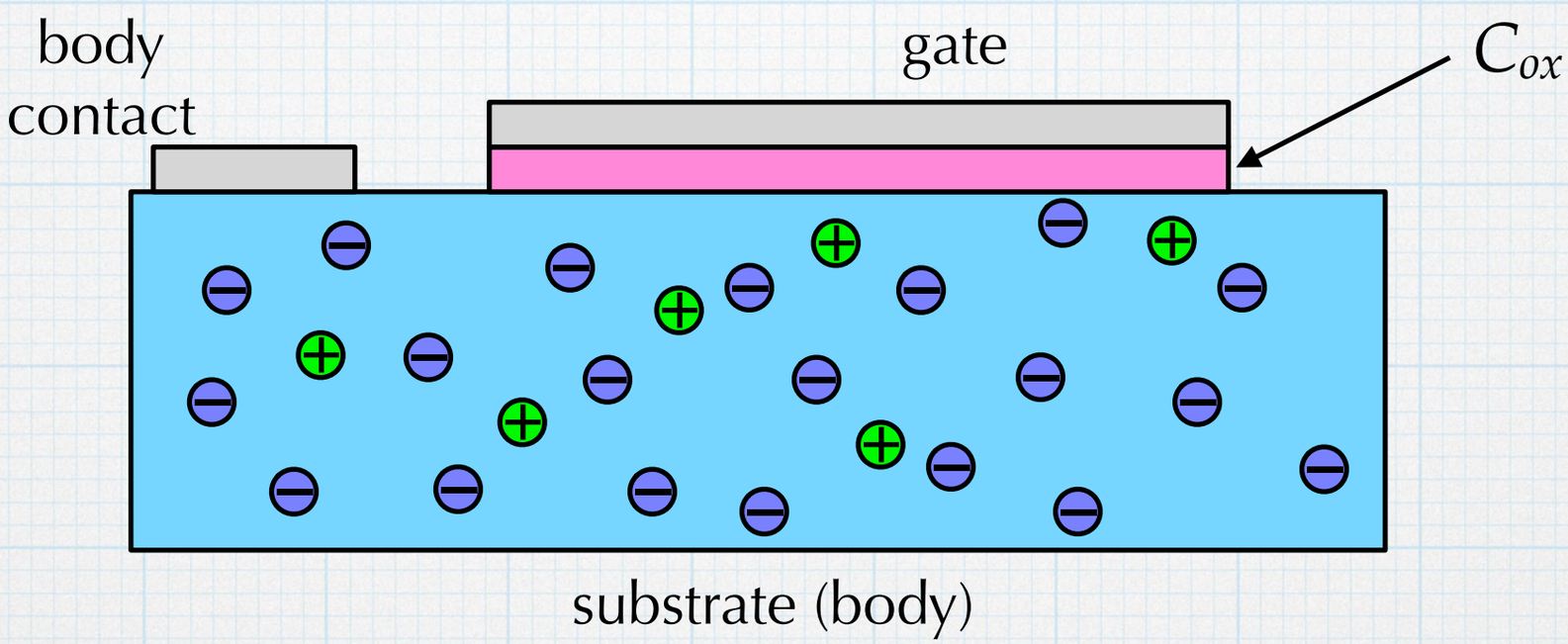
Apply a voltage between drain and source (V_{DS}) – there is always as reverse-biased diode blocking current flow.



To make current flow, we need to create a hole inversion layer.

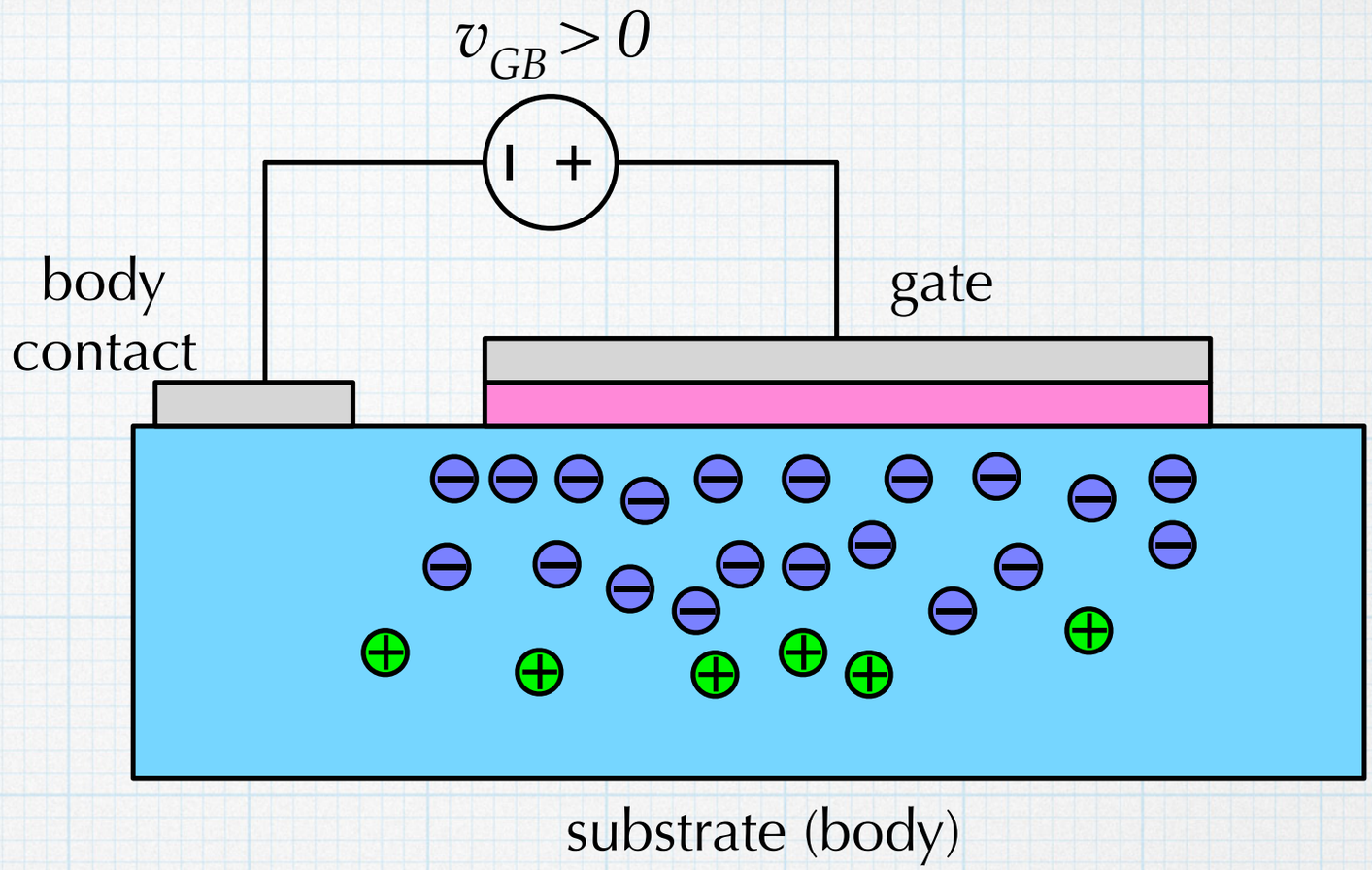
The PMOS capacitor

Same as the NMOS capacitor, but with *n*-type substrate.

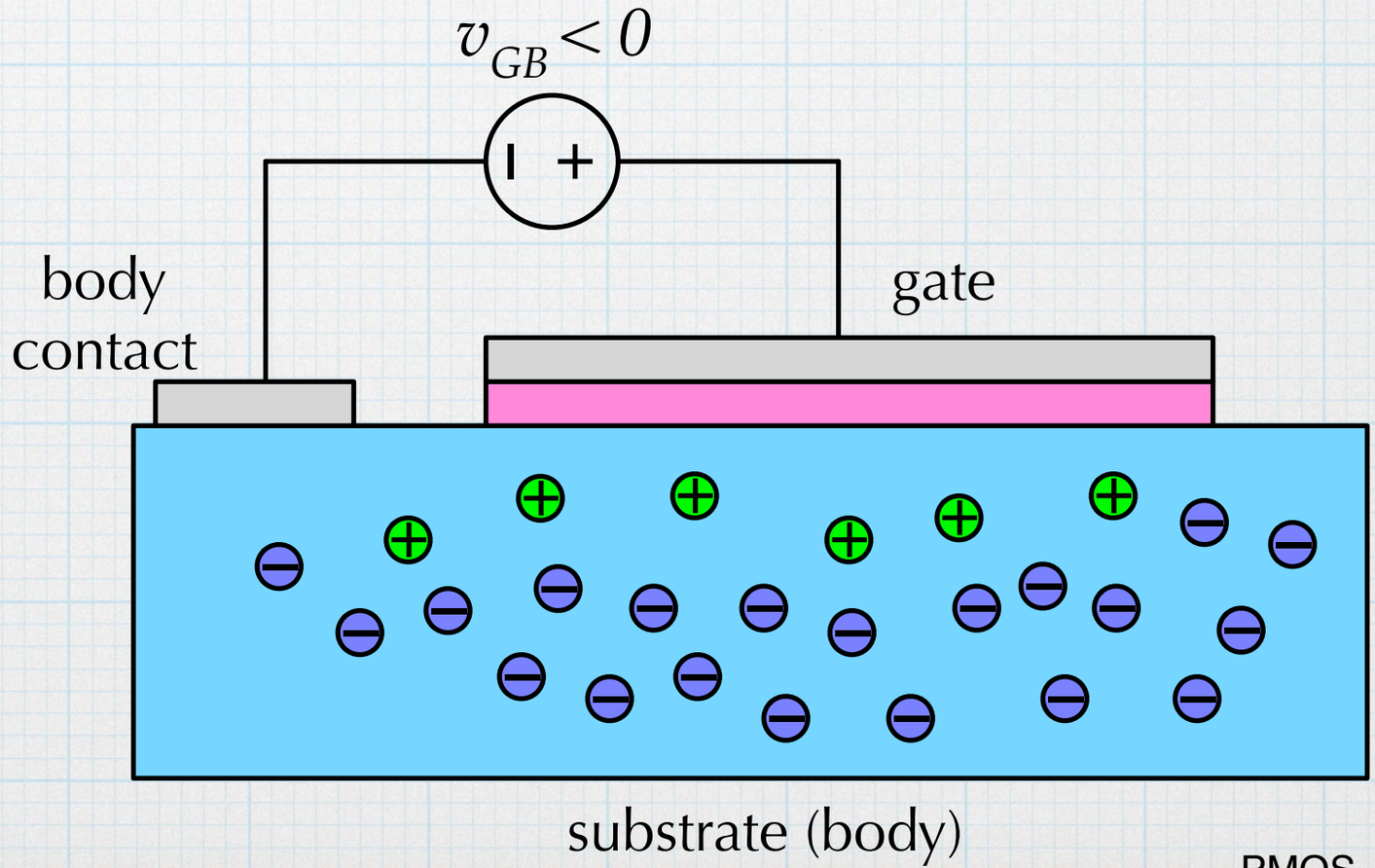


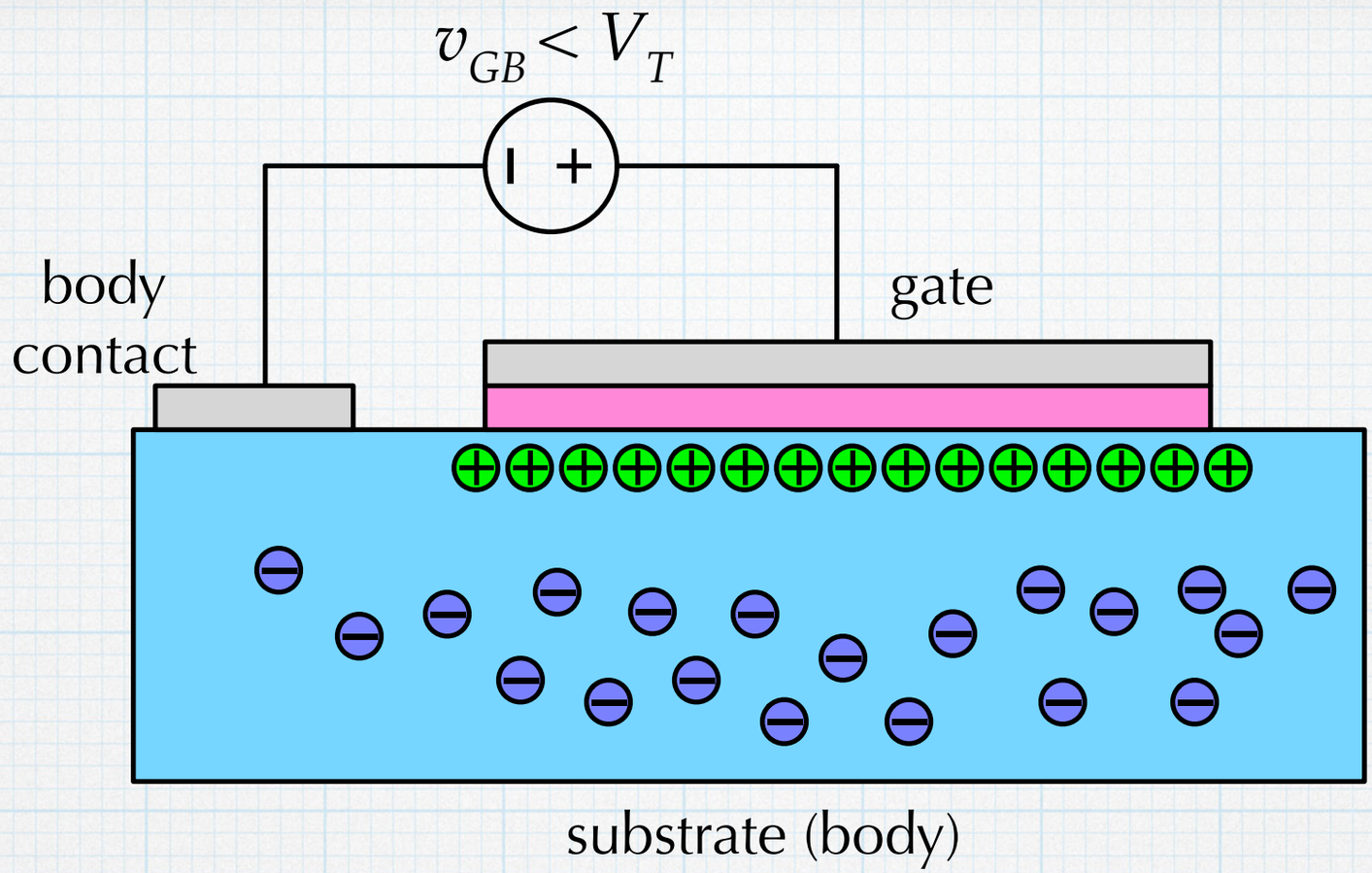
In the substrate, there are lots of electrons (majority carriers), and relatively few holes (minority carriers).

Apply a positive voltage to the gate – *electron accumulation*.



Apply a (smallish) negative voltage to the gate. Electrons are pushed away and a few holes are attracted – *carrier depletion*.





Applying increasing negative voltages to the gate causes more and more holes to pile up in a sheet underneath the oxide. At some particular voltage, the hole concentration in the sheet will be just as big as the electron concentration in the rest of the substrate. This is *hole inversion* and the voltage needed to create the inversion layer is the threshold voltage for the PMOS.

For PMOS, the threshold voltage is negative.

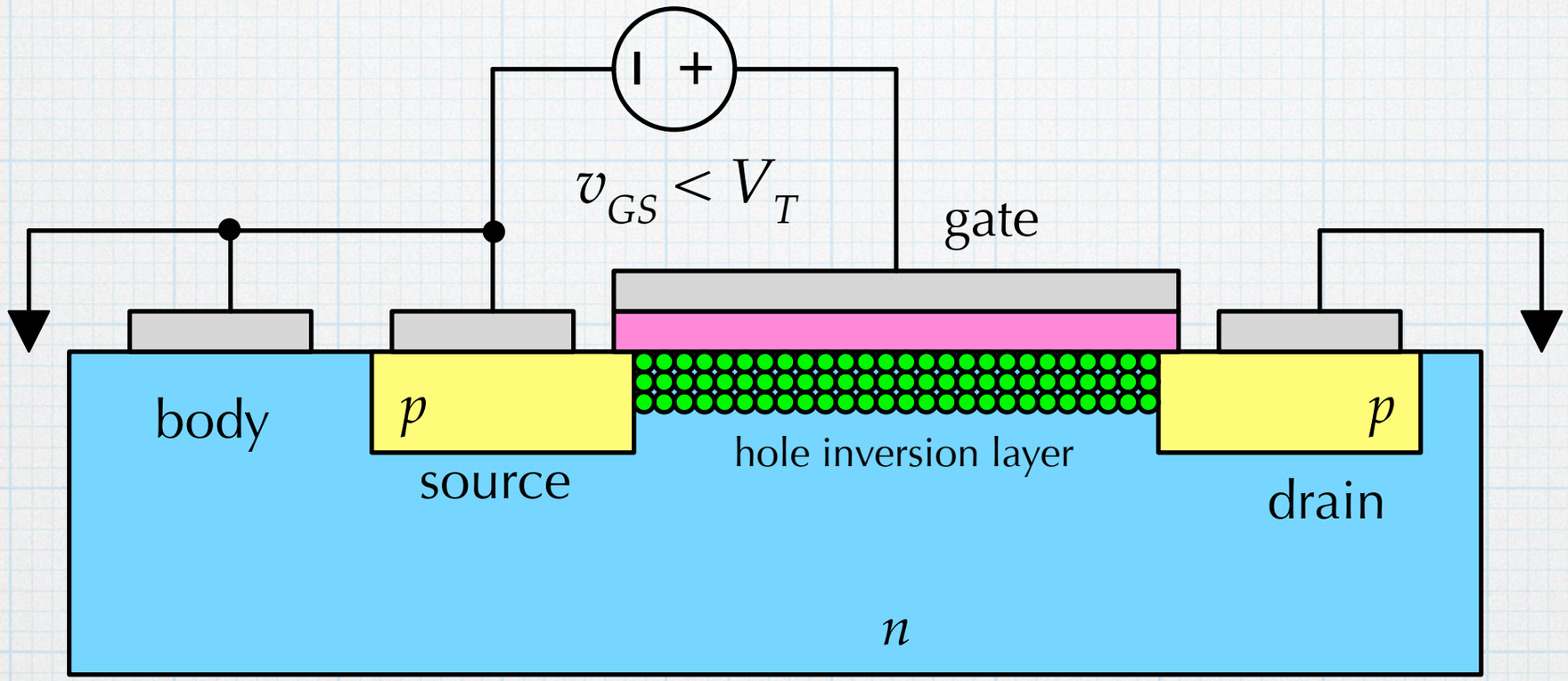
Making v_{GB} even more negative simply increases the hole concentration in the sheet.

Summary of PMOS capacitor operation

Through the application of the gate voltage, we can control what is happening with carriers under the gate.

$v_{GB} > 0$	electron accumulation
$V_T < v_{GB} < 0$	carrier depletion
$v_{GB} < V_T$	inversion – hole sheet forms. (Note: V_T is negative.)

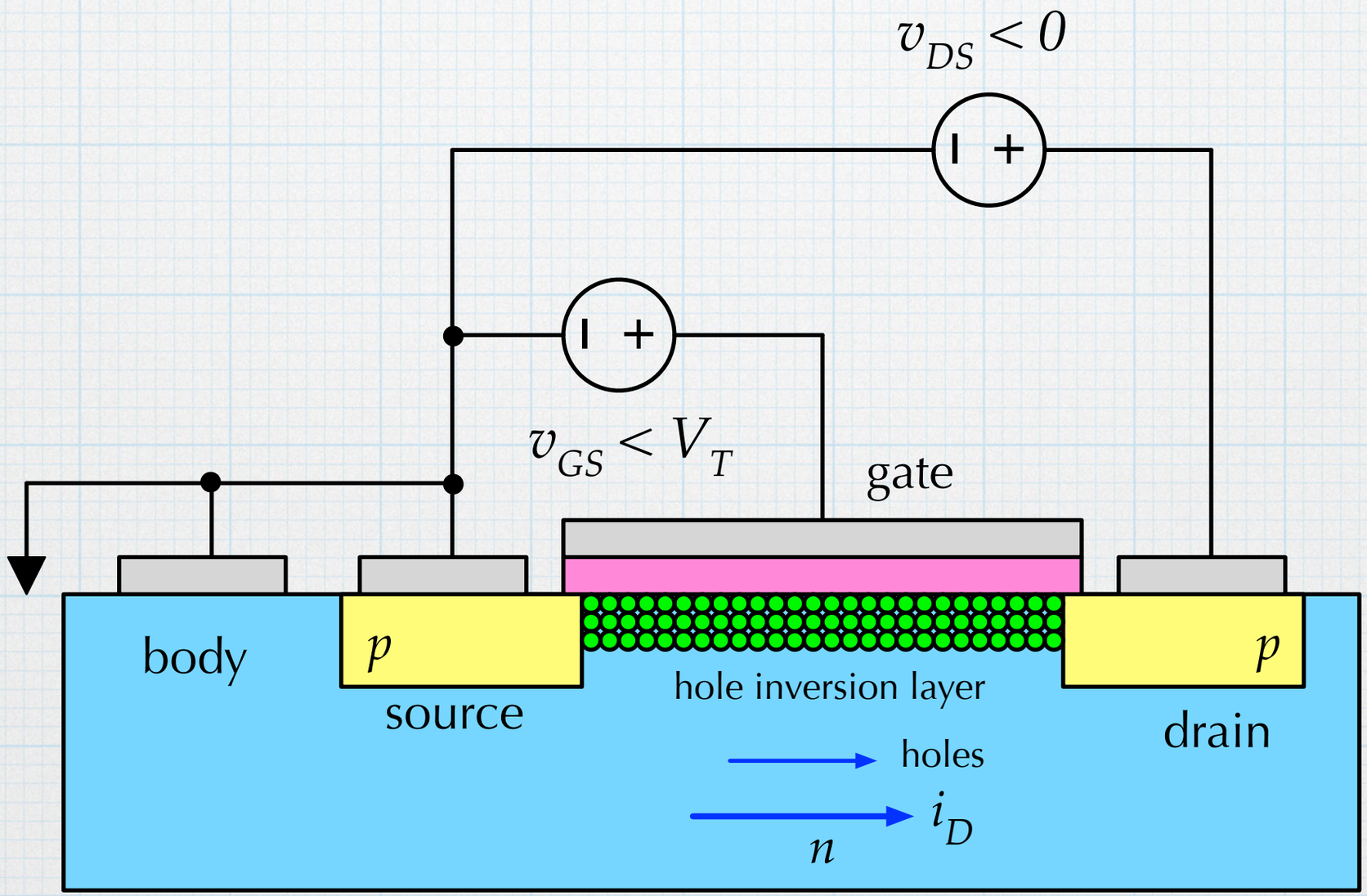
Creating a hole inversion layer connects the source to the drain. The PMOS is "on".

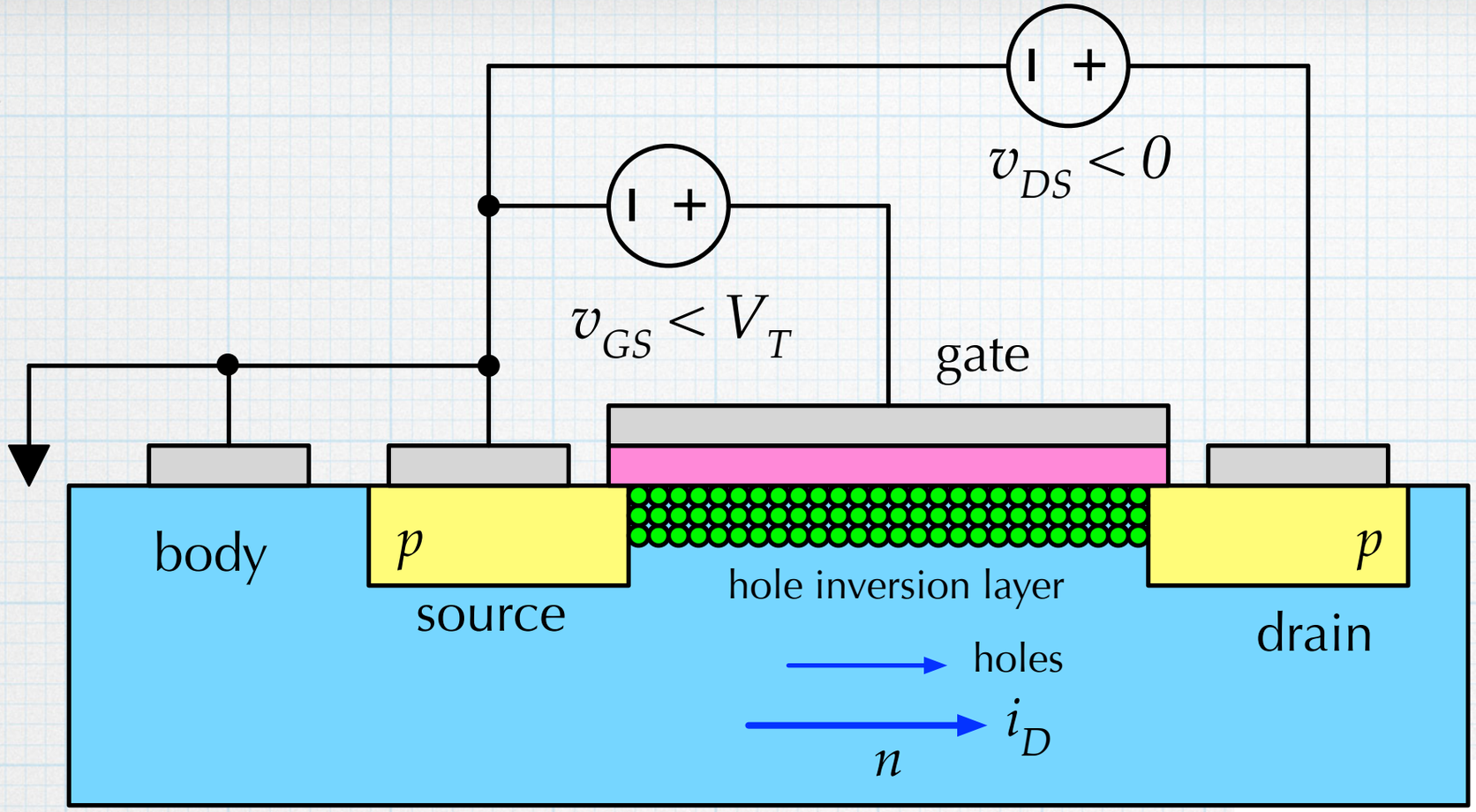


For now, we connect the source to the body and apply the controlling voltage between the gate and the source. This is OK for the time being, but we will have to revisit the issue of the body connection later. With the drain also at ground, the inversion layer (channel) is uniform between source and drain.

Drain current

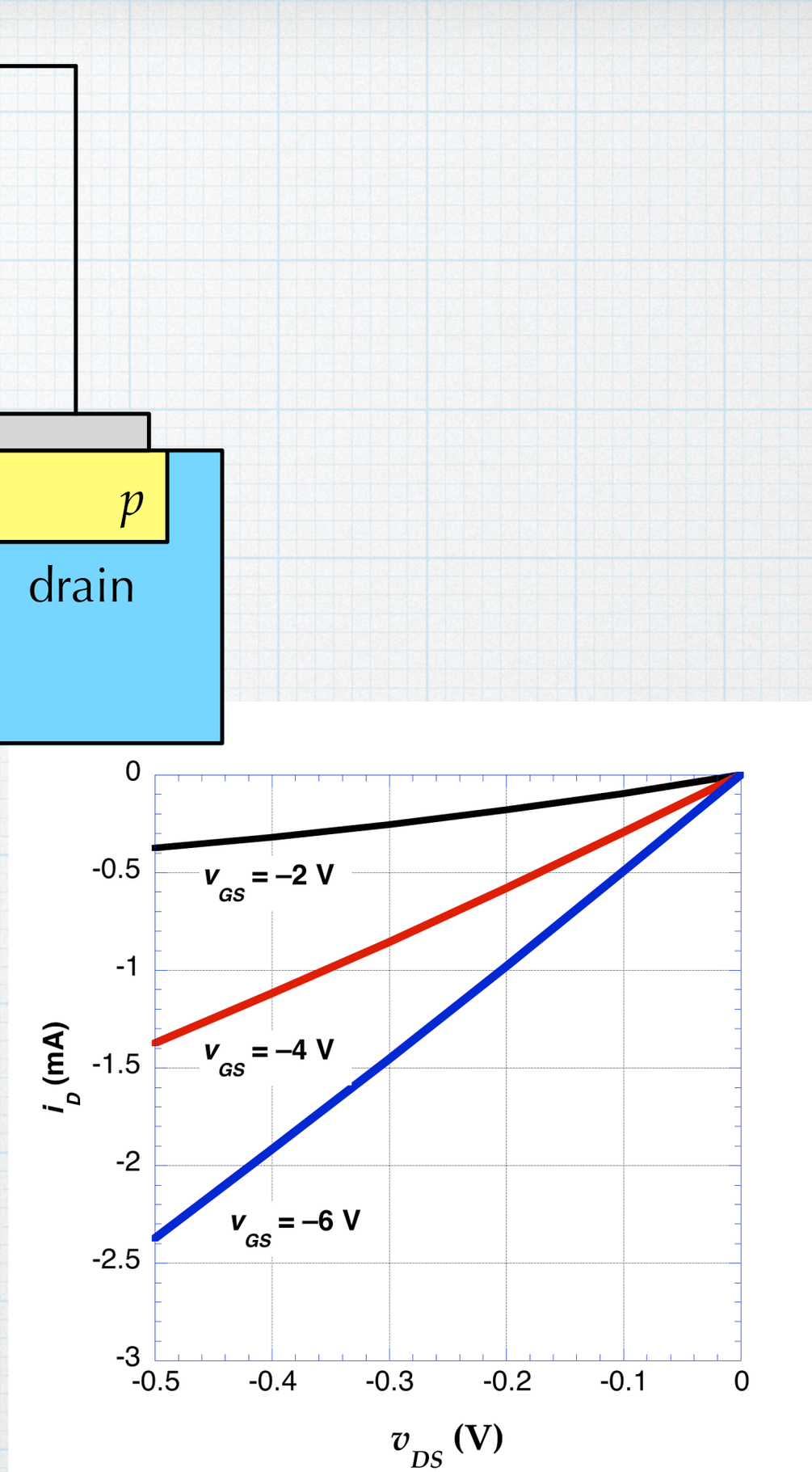
With the hole inversion layer formed ($v_{GS} < V_T$), current can flow by applying a *negative* voltage at the drain. This creates an electric field that will push holes from the source, through the inversion layer channel, and on into the drain. The moving holes represent a drain current flowing from source to drain. (Opposite the current for an NMOS!)

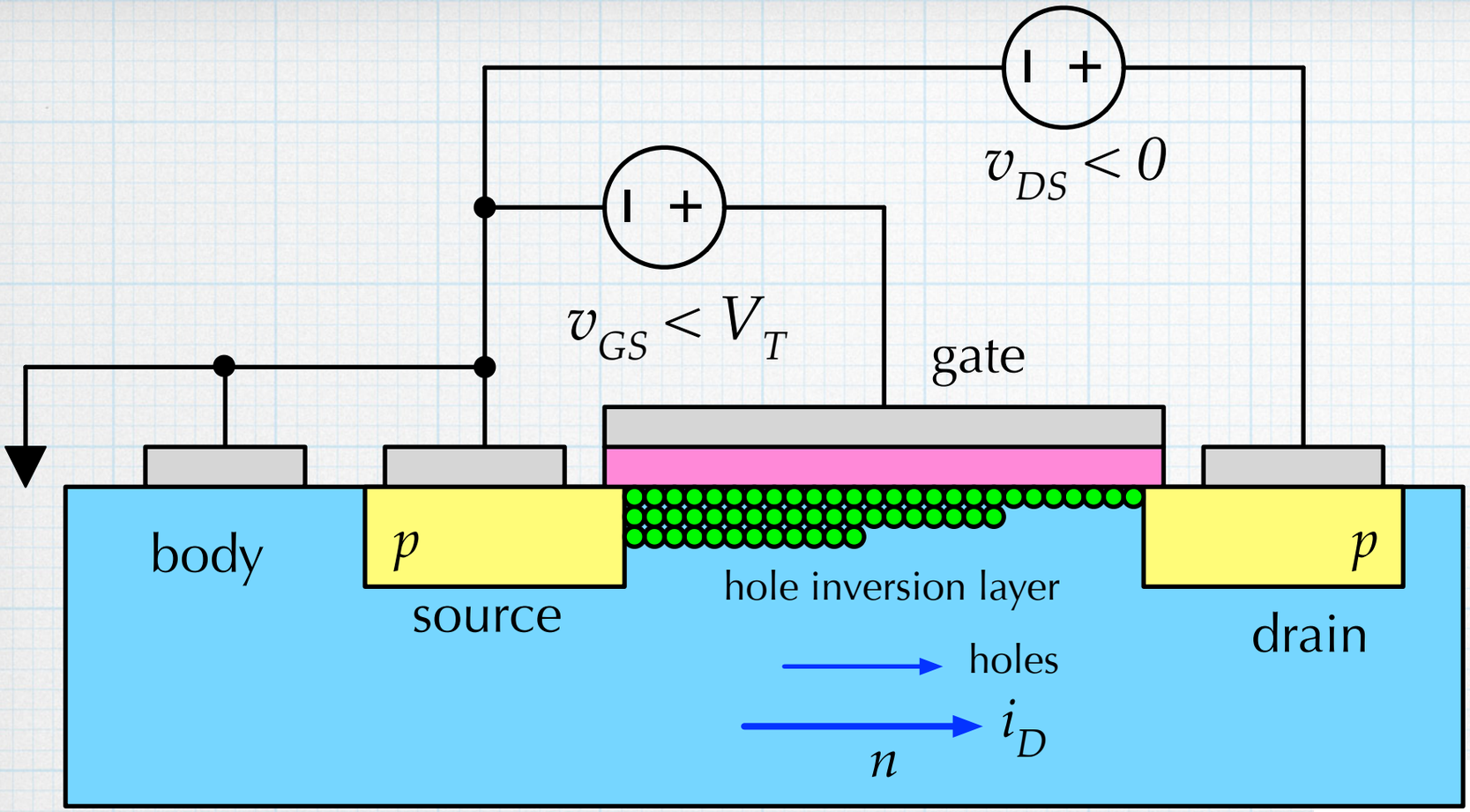




If v_{DS} is kept small, the current flow is "ohmic" – like a resistor. R_{DS} depends on the how much gate voltage is applied (determining the hole concentration in the inversion layer) and the physical dimensions of the PMOS.

$$i_D \approx \frac{v_{DS}}{R_{DS}}$$

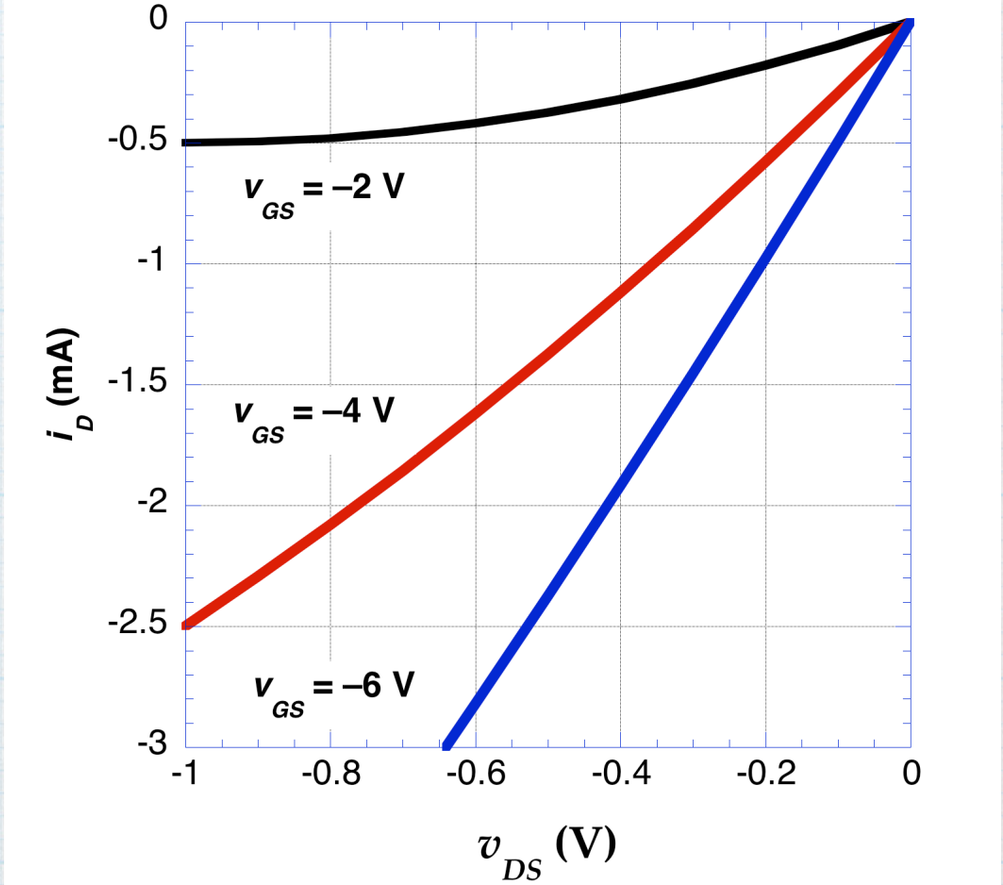


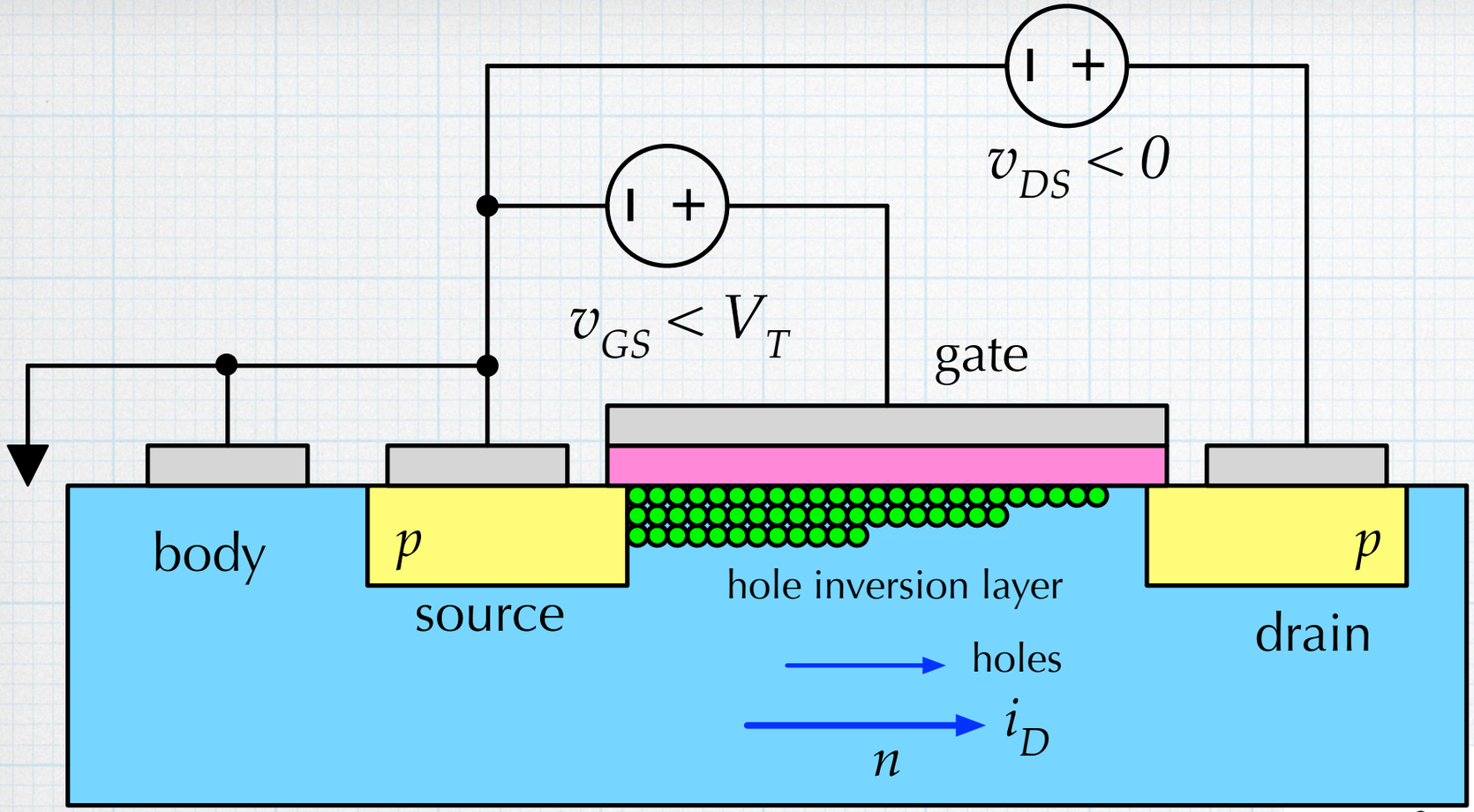


But as v_{DS} becomes more negative, the hole concentration at the drain is reduced – the channel is no longer uniform and it is becoming more resistive. The i-v curve becomes non-linear, becoming parabolic.

$$i_D = K\left[2\left(v_{GS} - V_T\right)v_{DS} - v_{DS}^2\right]$$

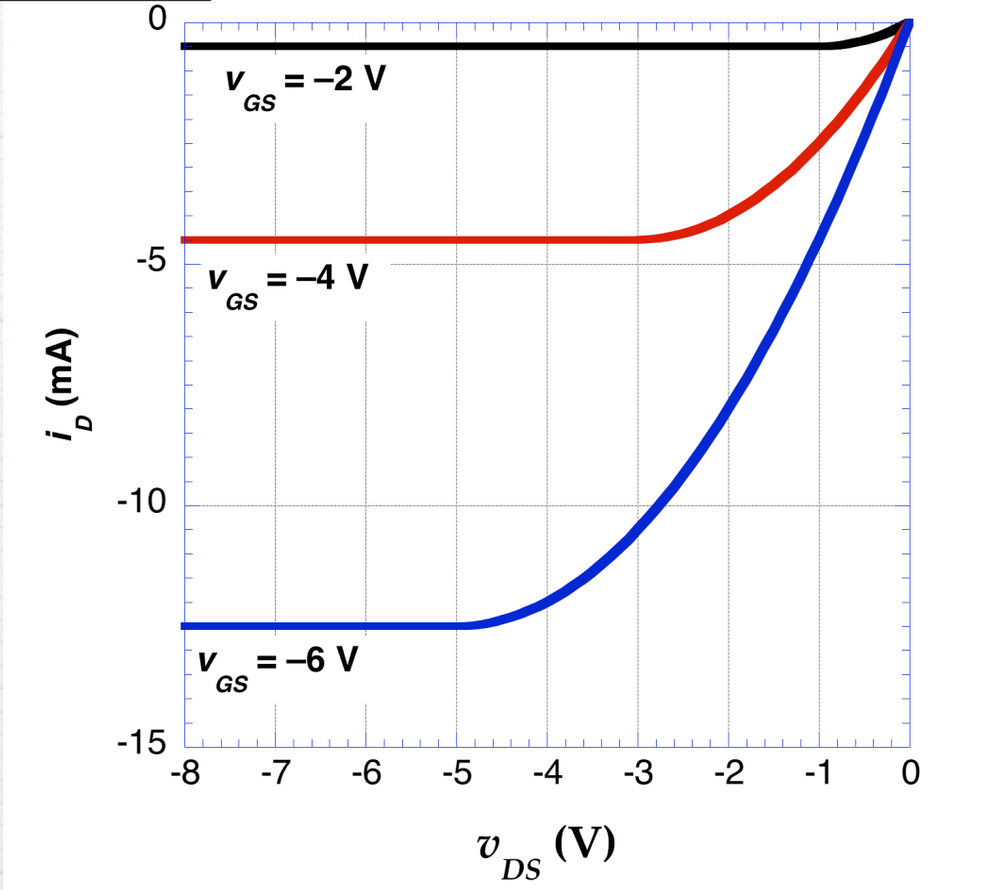
$$K = \frac{1}{2}\mu C_{ox}\frac{W}{L}$$





At sufficiently negative values for vDS, the channel becomes "pinched down" to its minimum possible value. Then the current saturates. The pinch-down occurs when $v_{DS} < v_{GS} - V_T$. Then the current in saturation is given by:

$$i_D = K\left[v_{GS} - V_T\right]^2$$



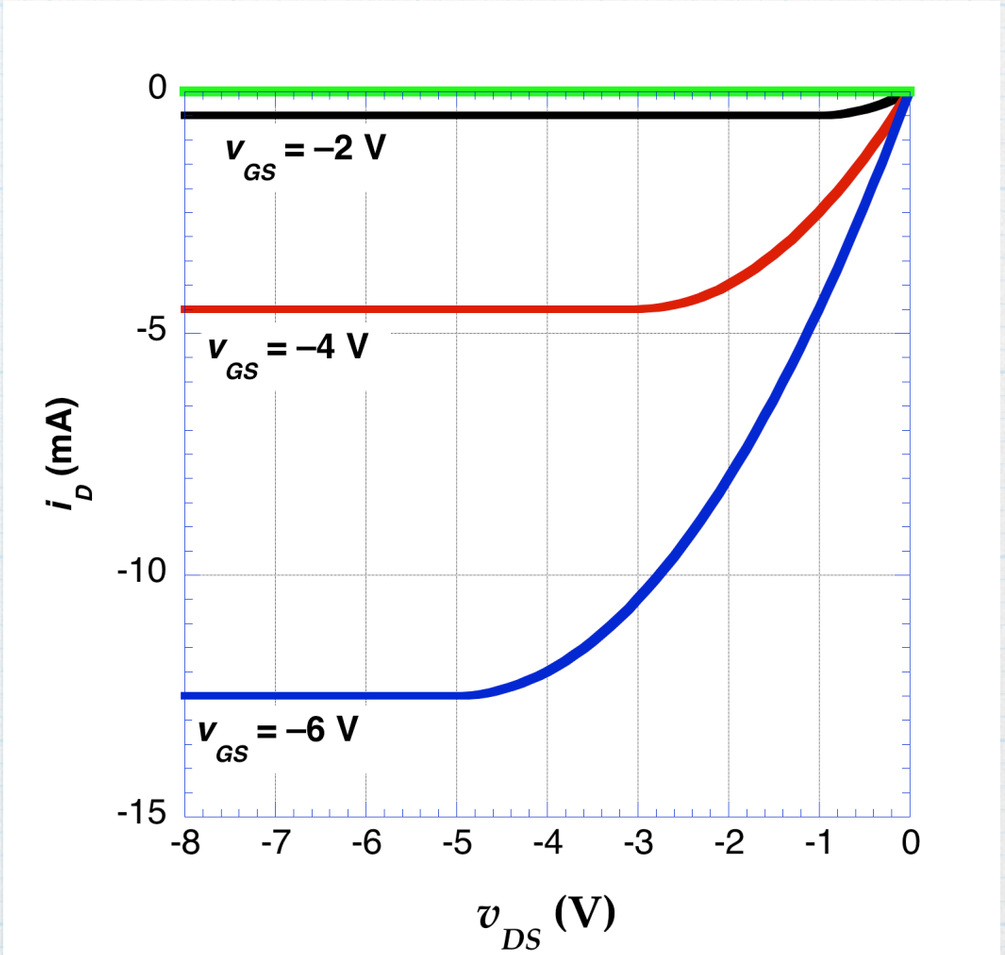
Summary of PMOS equations

$v_{GS} > V_T$	$i_D = 0$	off
$v_{GS} < V_T$ $v_{DS} > v_{GS} - V_T$	$i_D = K[2(v_{GS} - V_T)v_{DS} - v_{DS}^2]$	ohmic or linear
$v_{GS} < V_T$ $v_{DS} < v_{GS} - V_T$	$i_D = K[v_{GS} - V_T]^2$	saturation

$$K = \frac{1}{2}\mu C_{ox}\frac{W}{L}$$

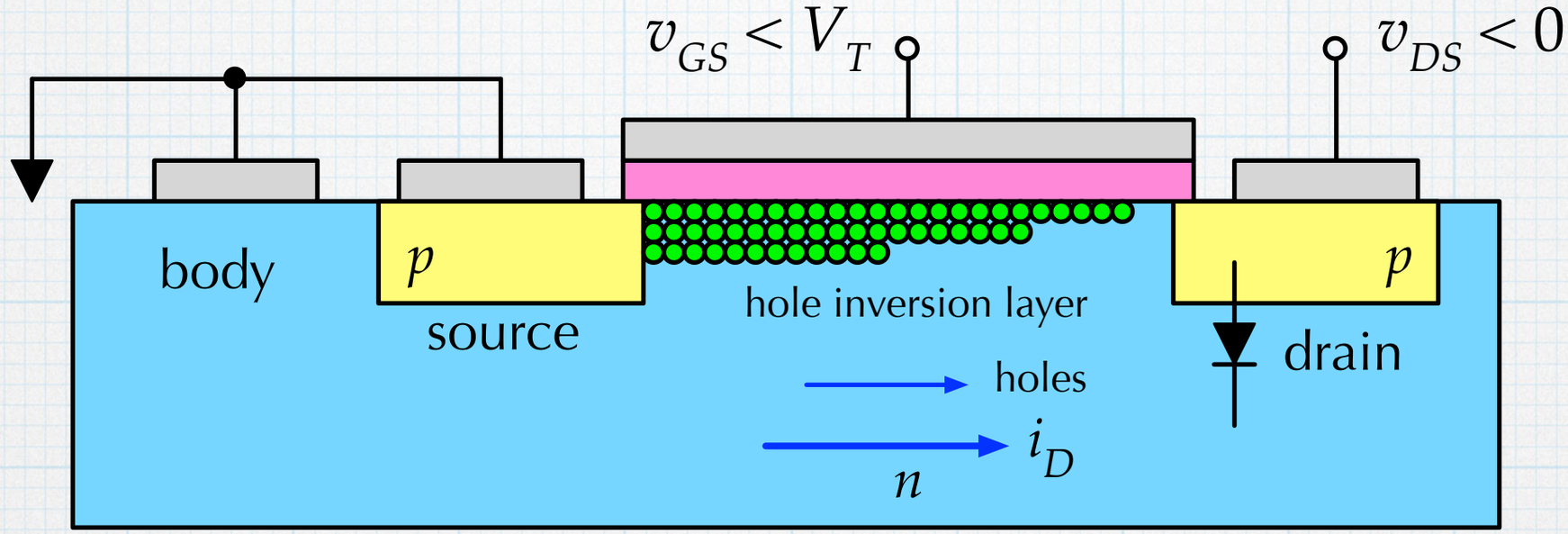
$$V_T < 0$$

Note the equations are identical to the NMOS equations. For a PMOS, v_{GS} and v_{DS} are both negative and the current flows from source to drain.



The PMOS substrate (body)

In applying the drain voltage to make the drain current flow, why did we use a negative value for v_{DS}? It would seem that a positive v_{DS} would be OK.



The reason becomes clear when we consider the p-n junction formed by the drain and the substrate.

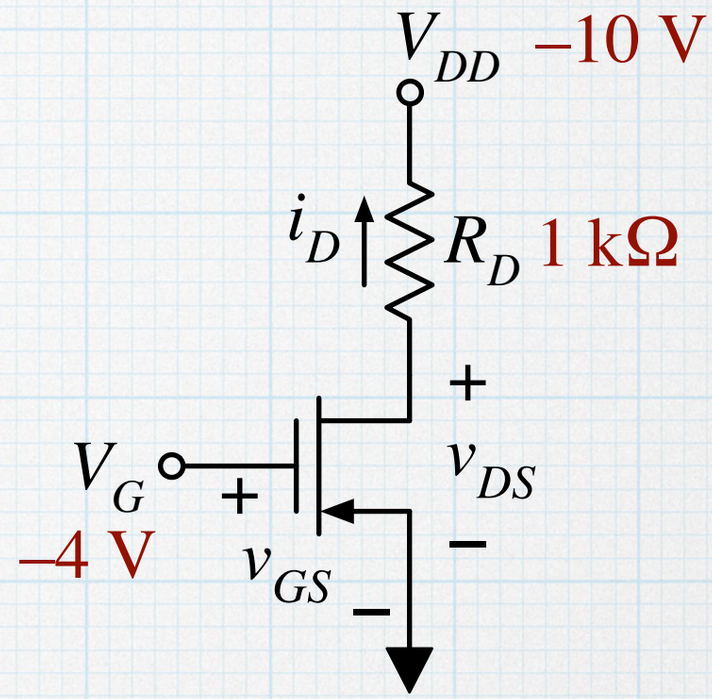
If the substrate is at ground potential and we apply a positive voltage to the drain, the p-n junction there would be forward-biased – probably with a very large voltage – and huge currents would flow from the drain into the substrate. The junction would likely be burned out.

The PMOS substrate rule: The substrate (body) should be connected to the highest voltage in the circuit – usually the positive power supply. Then the source and drain must both be at the same or lower voltages, and it will be impossible to forward-bias the diodes.

PMOS example

Since a PMOS is essentially an NMOS with negative voltages and current that flows in the opposite direction, it might seem reasonable that PMOS circuits would look like NMOS circuits, but with negative source voltages.

In the PMOS circuit at right, calculate i_D and v_{DS}.



In the circuit, $V_{GS} = -4$ V, which is more negative than the threshold voltage, so the PMOS must be on. Guess saturation:

$$i_D = K_p\left(v_{GS} - V_{Tp}\right)^2 = \left(0.5\,\text{mA/V}^2\right)\left[4\,\text{V} - 1\,\text{V}\right]^2 = 4.5\,\text{mA}$$

$v_{DS} = V_{DD} + i_D R_D$ (Be careful with signs!! Use KVL correctly.)

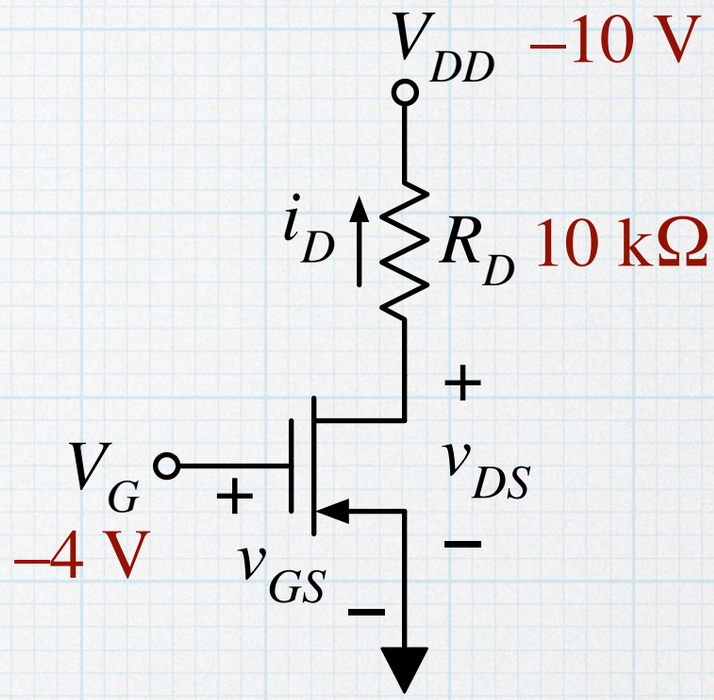
$$= -10\,\text{V} + \left(4.5\,\text{mA}\right)\left(1\,\text{k}\Omega\right) = -5.5\,\text{V}$$

V_{DS} is more negative than $V_{GS} - V_T$ ($= -3$ V), so saturation is confirmed.

PMOS example

Essentially the same circuit but with a different value of R_D.

From the previous examples, we can be certain that the PMOS is on. Guess saturation again, and we get the same value for the current.



$V_{TP} = -1\,\text{V}$

$K_p = 0.5\ \text{mA/V}^2$

$$i_D = K_p\left(v_{GS} - V_{Tp}\right)^2$$

$$= \left(0.5\,\text{mA/V}^2\right)\left[4\,\text{V} - 1\,\text{V}\right]^2 \quad = 4.5\,\text{mA}$$

$$v_{DS} = V_{DD} + i_D R_D \quad = -10\,\text{V} + \left(4.5\,\text{mA}\right)\left(10\,\text{k}\Omega\right) = 35\,\text{V}$$

Oh no! The drain-to-source voltage is not more negative than $V_{GS} - V_T$, so it can't be in saturation. In fact, 35 V is not even possible given the power supplies. The PMOS must be operating in ohmic.

$$i_D = K_p\left[2\left(V_{GS} - V_{Tp}\right)V_{DS} - V_{DS}^2\right]$$

$$v_{DS} = V_{DD} + i_D R_D$$

$$i_D = \frac{v_{DS} - V_{DD}}{R_D}$$

Equating the resistor current to the drain current:

$$\frac{v_{DS} - V_{DD}}{R_D} = K_p \left[2\left(V_{GS} - V_{Tp}\right) v_{DS} - v_{DS}^2 \right] \qquad \text{Blerk!}$$

Plug into your calculator and solve. Or do it the old-fashioned way — start by re-arranging:

$$v_{DS}^2 + \left[2\left(V_{GS} - V_{Tp}\right) - \frac{1}{K_p R_D} \right] v_{DS} - \frac{V_{DD}}{K_p R_D} = 0$$

Plug in values:

$$v_{DS}^2 + \left\{ 2\left[-4\,\text{V} - (-1\,\text{V})\right] - \frac{1}{\left(0.5\,\text{mA/V}^2\right)\left(10\,\text{k}\Omega\right)} \right\} v_{DS} - \frac{-10\,\text{V}}{\left(0.5\,\text{mA/V}^2\right)\left(10\,\text{k}\Omega\right)} = 0$$

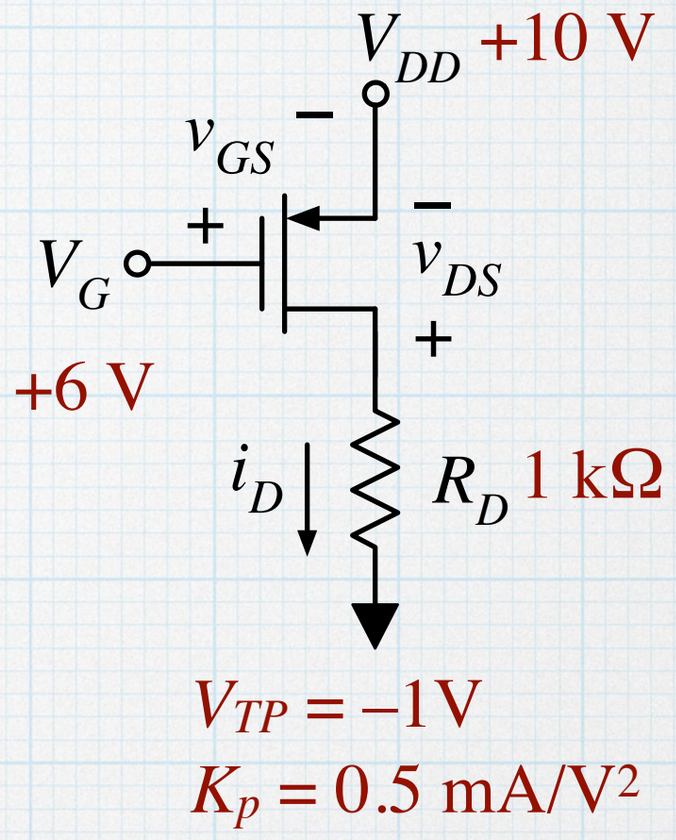
$$v_{DS}^2 + \left(-6.2\,\text{V}\right) v_{DS} + 2\,\text{V}^2 = 0$$

Solve to get $v_{DS} = -0.341$ V or $v_{DS} = -5.86$ V. The larger value is not consistent with the PMOS being in ohmic. So with $v_{DS} = -0.341$ V, the drain current is:

$$i_D = \frac{v_{DS} - V_{DD}}{R_D} = \frac{-0.341\,\text{V} - (-10\,\text{V})}{10\,\text{k}\Omega} = 0.97\,\text{mA}$$

PMOS example

However, we rarely use PMOS transistors with negative supplies as was done in the previous two examples. Typically PMOSs and NMOSs are used together, sharing the power supplies. To a PMOS with positive power supplies, we "flip it over" and use it "upside down" as shown the circuit at right.



Note the location of the gate, drain, and source and the corresponding voltages. Also the current flows "down".

$$v_{GS} = V_G - V_{DD} = 6\,\text{V} - 10\,\text{V} = -4\,\text{V}$$

$$v_{DS} = i_D R_D - V_{DD}$$

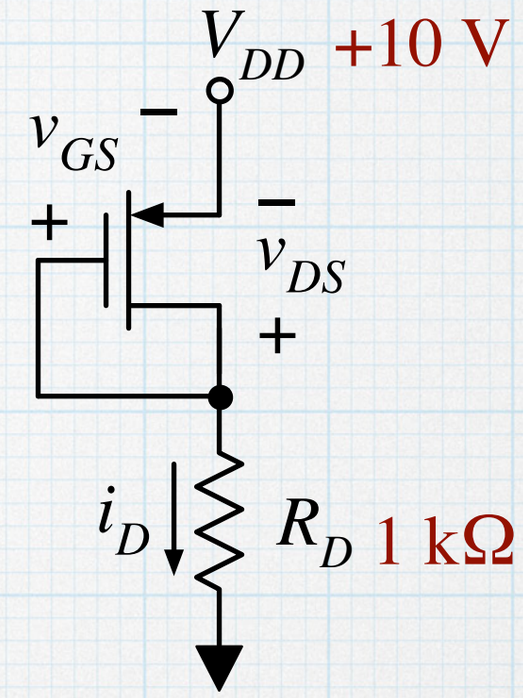
Guess saturation.

$$i_D = K_p\left(v_{GS} - V_{Tp}\right)^2 = \left(0.5\,\text{mA/V}^2\right)\left[4\,\text{V} - 1\,\text{V}\right]^2 = 4.5\,\text{mA}$$

$$v_{DS} = \left(4.5\,\text{mA}\right)\left(1\,\text{k}\Omega\right) - \left(10\,\text{V}\right) = -5.5\,\text{V} \quad \rightarrow \text{Saturation confirmed.}$$

PMOS example

With NMOS transistor, we saw that if the gate is tied to the drain (or more generally, whenever the gate voltage and the drain voltage are the same), the NMOS must be operating in saturation. The same is true for PMOSs. In the circuit at right, $v_{DS} = v_{GS}$, and so $v_{DS} < v_{DS} - V_{Tp}$ will always be true for $V_{Tp} < 0$.



$V_{TP} = -1\text{V}$

$K_p = 0.5\ \text{mA/V}^2$

With the PMOS in saturation:

$$i_D = K_p\left(v_{GS} - V_{Tp}\right)^2 = K_p\left(v_{DS} - V_{Tp}\right)^2$$

and,

$$v_{DS} = i_D R_D - V_{DD}$$

Insert the second into the first:

$$i_D = K_p\left(i_D R_D - V_{DD} - V_{Tp}\right)^2$$

Expand:

$$i_D = K_p\left[i_D^2 R_D^2 - 2\left(V_{DD} + V_{Tp}\right)\left(i_D R_D\right) + \left(V_{DD} + V_{Tp}\right)^2\right]$$

Re-arrange:

$$i_D^2 - \left[\frac{2\left(V_{DD}+V_{Tp}\right)}{R_D} + \frac{1}{K_p R_D^2}\right] i_D + \left[\frac{V_{DD}+V_{Tp}}{R_D}\right]^2 = 0$$

Plug in values:

$$i_D^2 - \left\{\frac{2\left[10\,\text{V} + (-1\,\text{V})\right]}{1\,\text{k}\Omega} + \frac{1}{\left(0.5\,\text{mA/V}^2\right)\left(1\,\text{k}\Omega\right)^2}\right\} i_D + \left[\frac{10\,\text{V} + (-1\,\text{V})}{1\,\text{k}\Omega}\right]^2 = 0$$

$$i_D^2 - (20\,\text{mA})\, i_D + 81\,\text{mA}^2 = 0$$

Solve to give: $i_D = 5.64$ mA or $i_D = 14.36$ mA. The larger voltage is too big — in that case $v_{DS} = +4.36$, which is not compatible for a PMOS. So the drain current is $i_D = 5.64$ mA and the corresponding drain-to-source voltage is $v_{DS} = -4.36$ V. All is good.